ACTIVE BALUN BASED ON OTA DEVICE

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MASTER OF ENGINEERING
IN
COMPUTER ENGINEERING

SCHOOL OF INFORMATION TECHNOLOGY
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Sittan Udomsom

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ABSTRACT

In modern communication systems, the signal splitter and combiner called BALUN (BALance to UNbalance) is required to interface a single ended device with a differential device. Most active BALUNs deploy passive elements which cannot be tuned and require large area in the integrated circuit. Though, there is the controllable BALUN based on BiCMOS CCCII, the implementing circuit is quite large in a transistor count and the cost of BiCMOS is very expensive. In this work, the new active BALUN based on CMOS OTA is proposed. By adjusting the transconductance of the composed OTAs, the characteristics of the BALUN can be tuned electronically. Normally, the size of the OTA is half of the size of the CCCII in the transistor count. Therefore, the size of the proposed structure is theoretically half of the CCCII counterpart. The design structure is simulated in the HSPICE based on the 90nm IBM RF-CMOS process parameters extracted by MOSIS. The result shows that the proposed structure can be a fair alternative in the BALUN design via adequate compatibility of the BALUN characteristics such as power-splitting, power-combination and phase inverting.

Keywords: Operational Transconductance Amplifier/ActiveBALUN/CMOS

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CHAPTER 1

INTRODUCTION

1.1 Background and Problem Definition

Nowadays, most transceivers are composed of both single ended (SE) and differential ended (DE) components. Therefore, a converter circuit called the BALanced to UNbalanced (BALUN) converter is usually needed. Most BALUN designs are based on passive components, BJT, and BiCMOS. Though these designs work well on their own, most transceivers are favored to be fabricated based only on complementary MOS (CMOS) to be placed among various digital functions. In addition, ability in tuning is also a good option in the BALUN to cover errors in gain matching that are likely to occur with quite high probability in practical systems. Interestingly, the operational transconductance amplifier (OTA) simulating voltage-controlled current source (VCCS) is one of the favorite active analogue devices because the transconductance can be tuned electronically via bias current. Therefore, key properties of its applications can be easily tuned via single or multiple bias current. In addition, the OTA is usually small compared to the current controlled current conveyor (CCCII) which formerly composes a tunable active BALUN. In this paper, the novel active nanoscale CMOS BALUN is proposed based on the OTAs. The proposed circuit will be easily placed in a mixed signal chip because it requires no passive elements and no different types of transistors.

1.2 Objective

To design and simulate a new active BALUN based on an OTA device using AMS 0.35u Si-GeBiCMOS and IBM 90nm 9RF CMOS MOSFET model.

1.3 Scope

1.3.1 The new active BALUN will be based on CMOS OTA.

1.3.2 The simulated MOSFET model is based on the AMS 0.35µ Si-GeBiCMOS and IBM 90nm 9RF CMOS.

1.3.3 Performance simulations will be conducted by the HSPICE.

1.4 Procedure

1.4.1 Study structures and characteristics of BALUN.

1.4.2 Study structures and characteristics of OTA.

1.4.3 Design an OTA active BALUN.

1.4.4 Simulate performance by the HSPICE.

1.4.5 Analyze results.

1.4.6 Adjust the design to fit the required performance.

CHAPTER 2

BACKGROUND THEORY AND LITERATURE REVIEW

2.1 Review of BALUN

A BALUN is a device for conversion between a single-ended signal and a differential signal. The differential signal can be considered as two signals with equal voltage but 180º antiphase. A high performance BALUN design is critical for integrating the single-ended and differentialsignals. Bandwidth, phase and magnitude imbalances are all the important issues in the BALUN design (Figure 2.1).

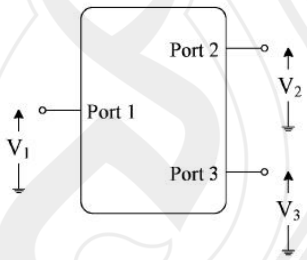


Figure 2.1 Basic Structure of BALUN

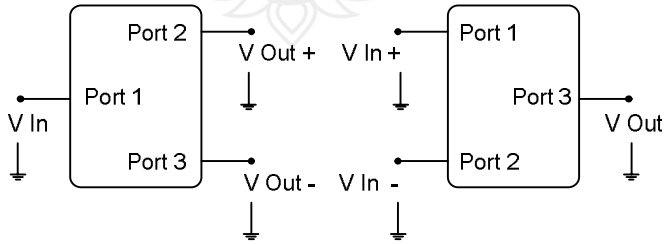


Figure 2.2 Power Split and Power Combined BALUN

2.1.1 Characteristic Parameters of BALUN

Consider the BALUN as a power splitter and combiner (Figure 2.2). Ideally, the signals at the two differential ports are equal in magnitude and 180° out of phase for all frequencies, but in practice, the magnitudes of differential output voltageare slightly different (amplitude imbalance), there exists a phase imbalancebetween the two output signals away from the ideal 180° difference. Generally, BALUNs are required to show 50-characteristic impedances at all the ports.

2.1.2 What is OTA?

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS) (Gnecchi, 2010). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

The ideal transfer characteristic is

$$\mathrm{I}_{\mathrm{out}} = g_m\left(V_{In+} - V_{in-}\right) \qquad (1)$$

Or, by taking the pre-computed difference as the input,

$$\mathrm{I}_{\mathrm{out}} = g_m V_{In} \qquad (2)$$

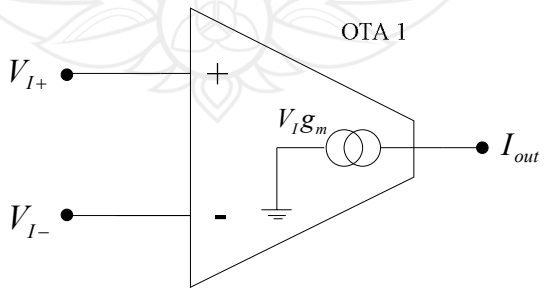


Figure 2.3 Schematic Symbols for the OTA.

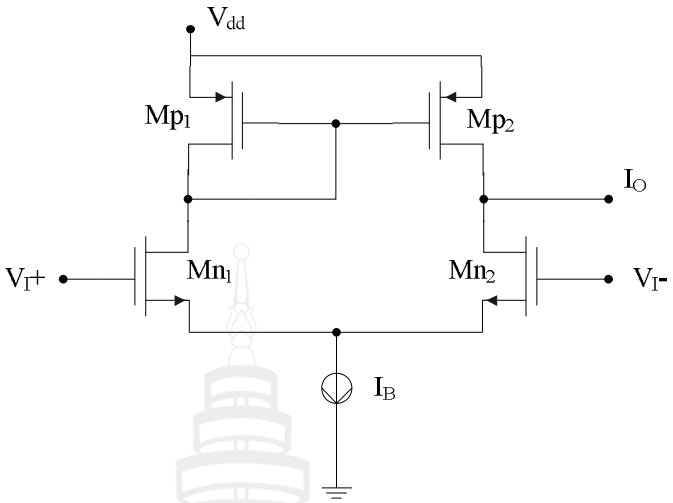


Figure 2.4 Transistor Level of Operational Transconductance Amplifier

For a new solution of BALUN,considering a schematic diagram of OTA device, the transistor level of the OTA is used in a positive part as shown in Figure 3.1. V_I+ and V_I- are applied to Mn_1 and Mn_2 as inputs of acircuit.

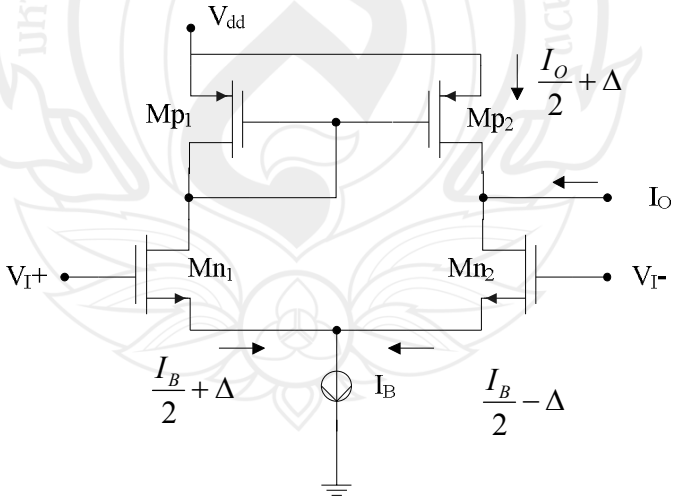


Figure 2.5 Transistor Level of OTA with Current Flow Path

From the current flow path in Figure 3.1,the current entering I_O is

$$I_O = \frac{I_B}{2} - \Delta - \frac{I_B}{2} - \Delta \qquad (3)$$

Therefore $$I_O = -2\Delta \qquad (4)$$

For an equivalent circuit model of an OTA

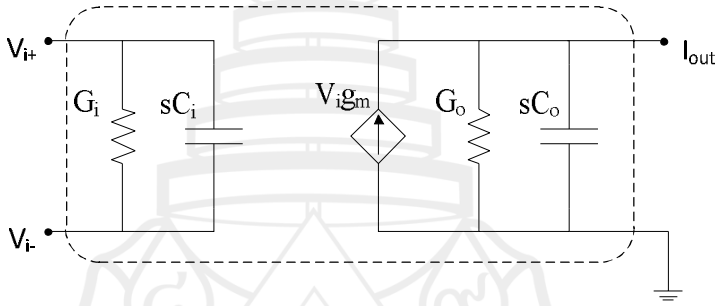


Figure 2.6 An Equivalent Circuit Model of Operational Transconductance Amplifier

2.2 Literature Review

2.2.1 Passive Element BALUN

The simple BALUN transformer was made by twisting a pair of magnets wired around ferrites. To make a single-ended signal on a primary side, a negative port was connected to ground and two secondary ports were connected todifferential inputs. With a characteristic of the transformer, BALUN could give an impedance transformation. A major problem of this type of BALUN was a larger size of incapacity.

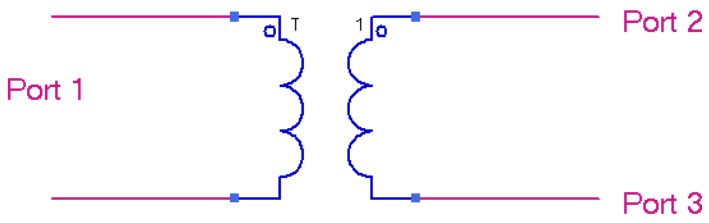
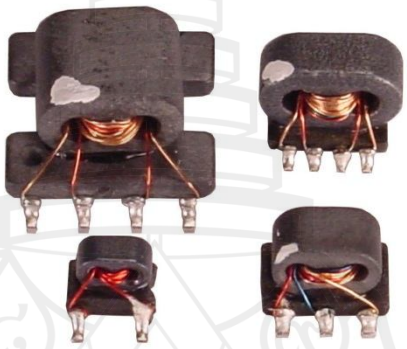
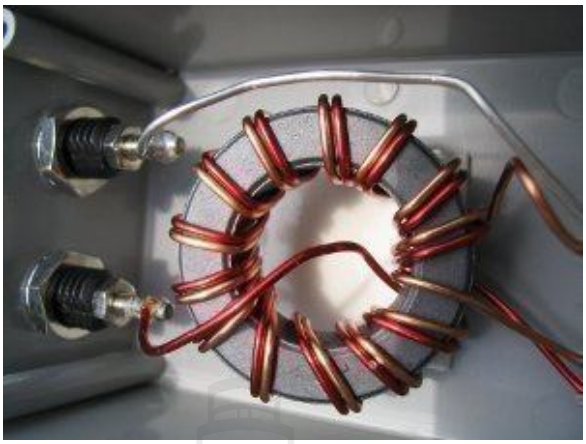


Figure 2.7 Electrical Symbolic of Transformer BALUN



From MPS Industries. (n.d.). **Balun transformers.** Retieved August 18, 2012, from http://www.mpsind.com/MPS-pages/MPS-product-pages/balun-transformers.html

Figure 2.8 R3838 SMT Mini Wideband Transformers 3.8mm x 5.0mm



From Wendell, R. J. (n.d.). **WBØJNR: My amateur radio station.** Retieved August 18, 2012, from http://www.rogerwendell.com/mystation.html

Figure 2.9 Transformer BALUN Balun Toroid

The second BALUN method was to use planar waveguides or microstrip transmission lines or coaxial cable BALUN. This type of BALUN provided bandwidth capability by using quarter-wave lines as long as the center frequencies, but requiring a large area for wavelengths.

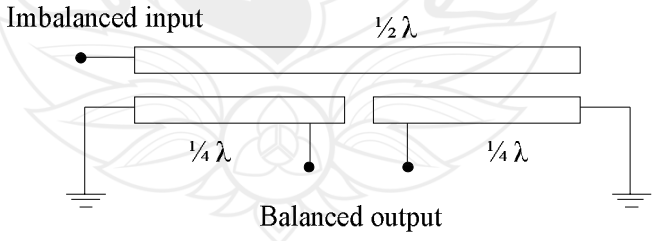


Figure 2.10 Basic Schematic of Waveguide BALUN

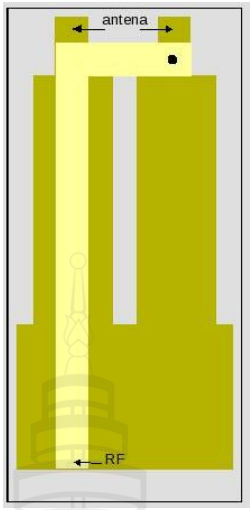
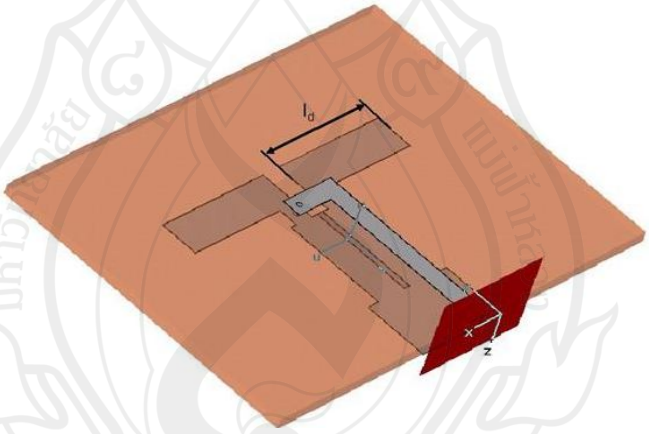


Figure 2.11 Microstrip Waveguide BALUN



From Chuang, H. R. & Kuo, L. C. (2003). 3-D FDTD Design Analysis of a 2.4-GHz Polarization-Diversity Printed Dipole Antenna with Integrated Balun and Polarization-Switching Circuit for WLAN and Wireless Communication Applications. **IEEE Transactions on Microwave Theory and Techniques, 51**(2), 374-381.

Figure 2.12 Microstrip Waveguide BALUN Built in with Dipole Antenna 2.10 and 2.11 Printed Dipole Antenna with Integrated Balun

The third one was called LRC Networks BALUN.There were benefits for small form factors and a high potential for integration, however, it could only be tuned in to a narrow band and sometimes unattainable to reduce imbalances due to being a passive device

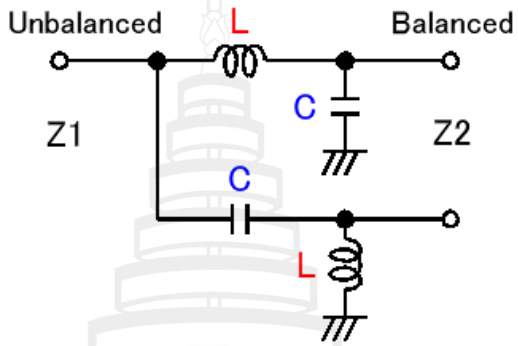


Figure 2.13 LRC Networks BALUN Narrowband BalunCalculator

2.2.2 Transistor Based BALUN

The simplest active implementation of BALUN is to use a single transistor (Figure 2.14).The inputs fed to the base and the differential signals are tapped at the collector and emitter. The input signals are applied to the base (Input) and the outputs are taken from both the emitter (+) and the collector (-) (Roozbahani, 2004). The phase output signals are correspondingly 180° from each other, and thus produce a balanced signal from an unbalanced one.

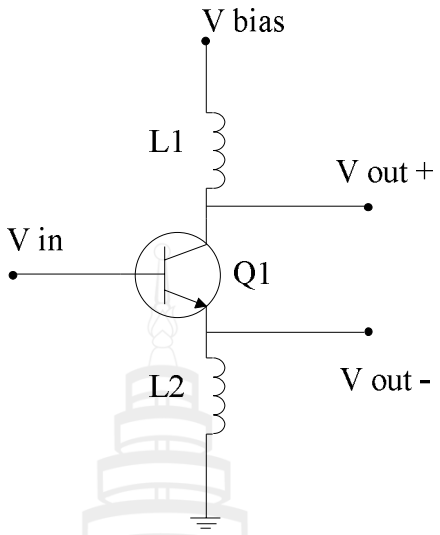


Figure 2.14 Single Transistor BALUN

The classic common-emitter differential pair (Baker, 2010). Can be converted to a BALUN by grounding one of the inputs through a capacitor.

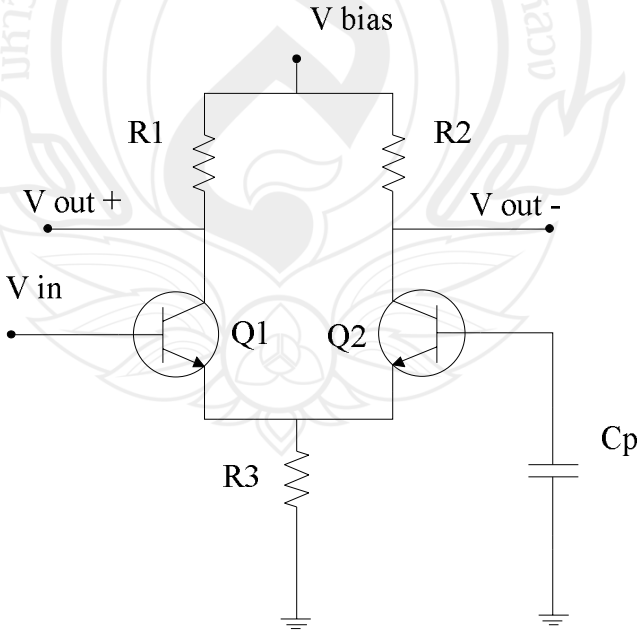
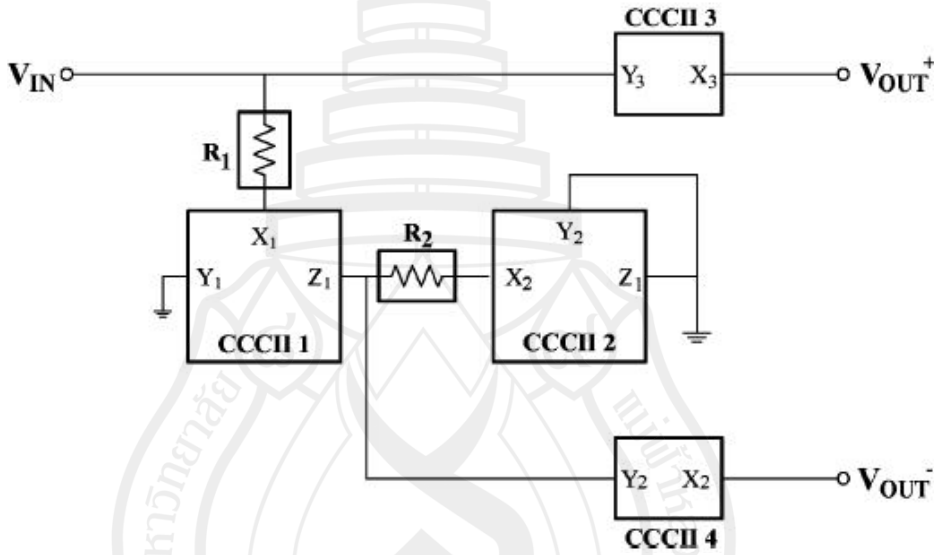


Figure 2.15 Differential Pair Transistor BALUN

2.2.3 CCCII BALUN

The second-generation current-controlled conveyor (CCCII) is a popular building block for analog electronics functions at baseband, RF, and video frequencies. The CCCII is composed of three input-output ports using BALUN (Godara & Fabre, 2007), and 4 blocks of the CCCII are in operation. The problem is the CCCII structure needs a large number of transistors and MOSs so this structure needs more area for chips, is expensive, and has more CMOS error problems from industrial lines.



From Godara, B. & Fabre, A. (2008). A highly compact active wideband balun with impedance transformation in SiGeBiCMOS. **IEEE Transactions on Microwave Theory and Techniques, 56**(1), 22-30.

Figure 2.16 Blocked Level of the CCCII-based BALUN

As previously mentioned, the passive BALUN needs a large space which varies inversely with frequency and is difficult to be adjusted to fit the required frequency, for example, transformer BALUN, wavelength BALUN and RLC BALUN. The problem can be solved by using an active BALUN circuit with a single

transistor or differential pair transistor which helps decrease the size of the circuit and is easier to be adjusted to fit the required frequency.

However, thereare still some limitations to how each type of transistors works based on its characteristics and quality (Cooke, 1971), including passive sessionsin the circuit because it cannot be used in high-frequency range or wide bandwidth. For less space of use, an active BALUN using a CCCII module is introduced asit needs much smaller space because it is fabricated on Bi-CMOS. The characteristics of the CCCII can make the BALUN used in wider frequency and the impedance adjusted to fit the required frequency.

Nevertheless, the structure of the CCCII is complicated because there are various types of transistors. This causes the fabricated procedure on the Bi-CMOS (Larson, 1998) to be more expensive and larger size than the active OTA BALUN presented in this research.

CHAPTER 3

PROPOSED METHOD

3.1 Power Split BALUN

To build a complete OTA active BALUN shown in Figure 3.1, OTA 1 and OTA 2 are used as power-splitter and anti-phase. OTA 3 and OTA 4 work as pre-load function to adjust the outputs.

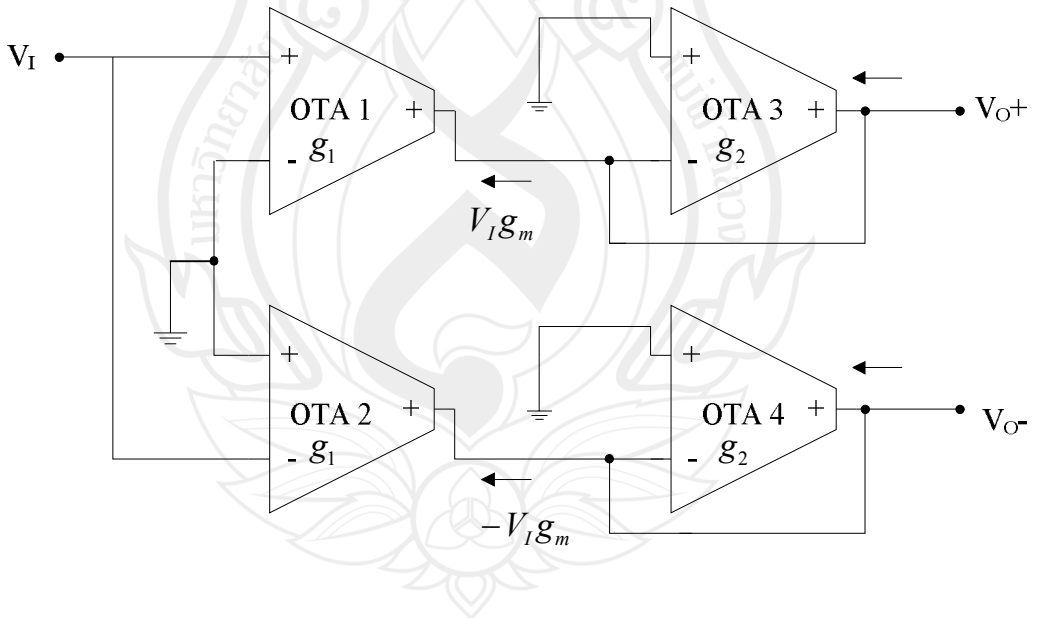


Figure 3.1 A Schematic of Active BALUN Using OTA

From Figure 3.1, the equation for V_O^+ is shown as follows:

$$V_I g_1 - V_O^+ g_2 = 0 \tag{5}$$

Therefore

$$V_O^+ = V_I \frac{g_1}{g_2} \tag{6}$$

For V_O^-

$$\left(-V_I g_1\right) + \left(-V_O^- g_2\right) = 0 \tag{7}$$

Therefore

$$V_O^- = -V_I \frac{g_1}{g_2} \tag{8}$$

From (10) and (12), V_O should be

$$V_O = V_I \left(\frac{2g_1}{g_2} \right) \tag{9}$$

Then

$$g_2 = 2g_1 \tag{10}$$

And

$$V_O \cong V_I \tag{11}$$

An equivalent circuit of power split BALUN is shown in Figure 3.2.

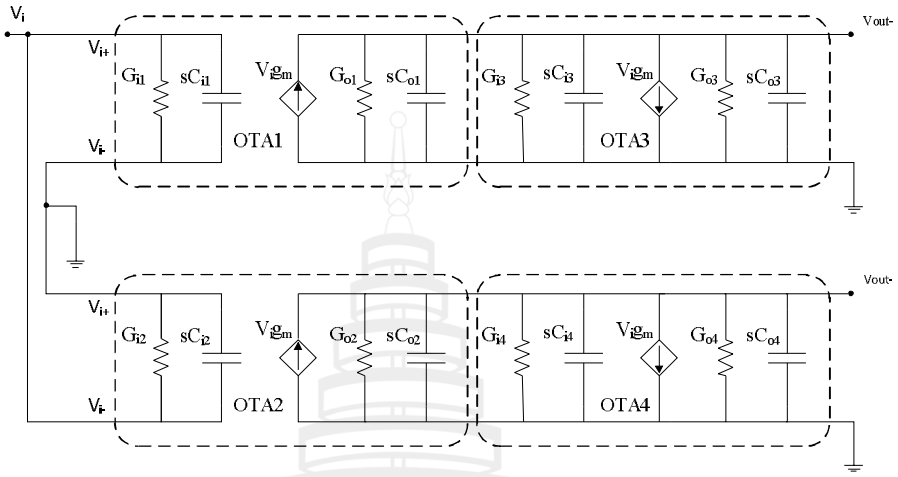


Figure 3.2 An Equivalent Schematic of Active BALUN

To calculate input impedance of power split BALUN connected voltage source to an input port and connect an output port to ground, then measure and calculate a voltage source current output or I_i

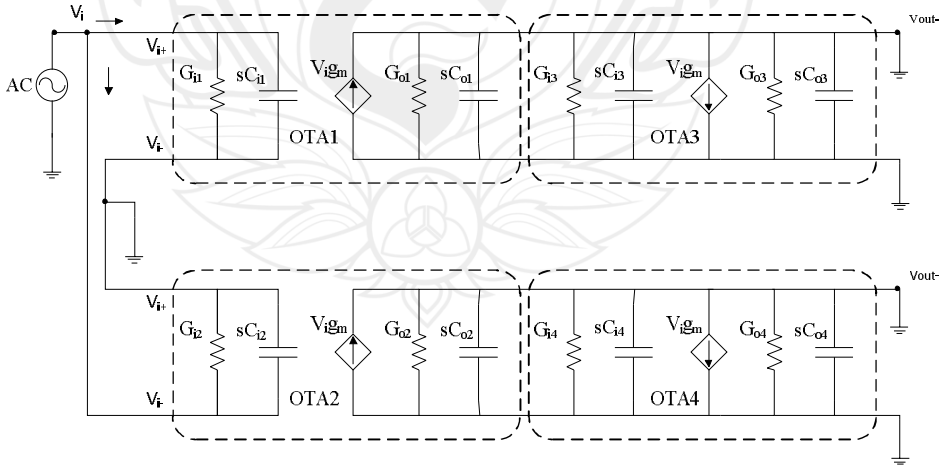


Figure 3.3 An Equivalent Schematic of Active BALUN (Connected Voltage Source to Calculate z Input Impedance)

Reduced to

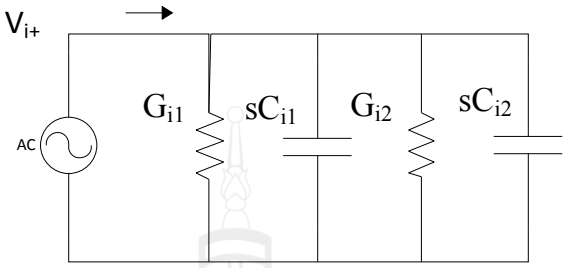


Figure 3.4 An Equivalent Schematic of Active BALUN (Reduced)

Assume that

$$G_{i_1} = G_{i_2} \tag{12}$$

And

$$sC_{i_1} = sC_{i_2} \tag{13}$$

So

$$I_i = V_i 2\left(G_i + sC_i\right) \tag{14}$$

Then

$$Z_{in} = \frac{V_i}{I_i} = \frac{1}{2G_i + s2C_i} \tag{15}$$

To calculate output impedance of each part by connecting positive outputs to a voltage current source, then negative outputs and inputs to ground.

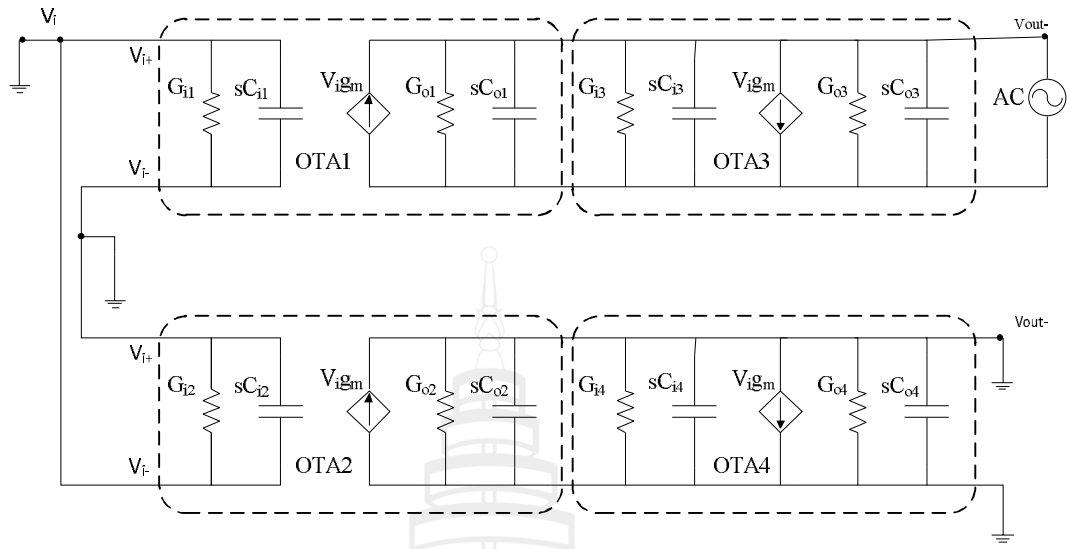


Figure 3.5 An Equivalent Schematic of Active BALUN (Connected Voltage Source to Calculate z Output Impedance)

Reduced to

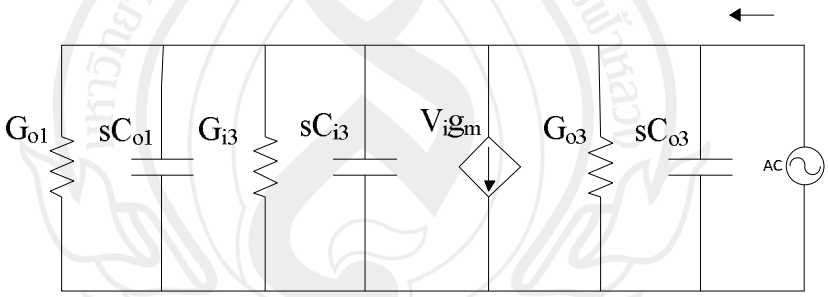


Figure 3.6 An Equivalent Schematic of Active BALUN (Reduced)

Then I is equal to

$$I_i = V_i\left(g_{m_2} + G_{i_3} + G_{0_1} + G_{0_3} + s\left(C_{i_3} + C_{o_1} + C_{o_3}\right)\right) \qquad (16)$$

So the output impedance should be

$$Z_{out} = \frac{1}{\left(g_{m_2} + G_{i_3} + G_{0_1} + G_{0_3} + s\left(C_i + C_{o_1} + C_{o_{32}}\right)\right)} \tag{17}$$

Or assume that $G_{i_3} + G_{o_1} + G_{o_3}$ are near to zero when compared g_{m_2} to

$$Z_{out} \cong \frac{1}{\left(g_{m_2} + s\left(C_{i_3} + C_{o_1} + C_{o_3}\right)\right)} \tag{18}$$

then the output voltage in each side can be calculated in the equivalent cuicuit

$$V_{o^{\pm}} = \frac{V_I(g_m + G_{I_1} + G_{I_2} + s\left(C_{I_1}\right)}{g_{m_2} + G_{O_1} + G_{O_2} + s\left(C_{I_2} + C_{O_1} + C_{O_2}\right)} \tag{19}$$

3.2 Power Combined BALUN

The structure for a signal combining BALUN is shown in Figure. 3.7. The OTA 1 is used as an input stage and the OTA 2 acts as a pre-load device.

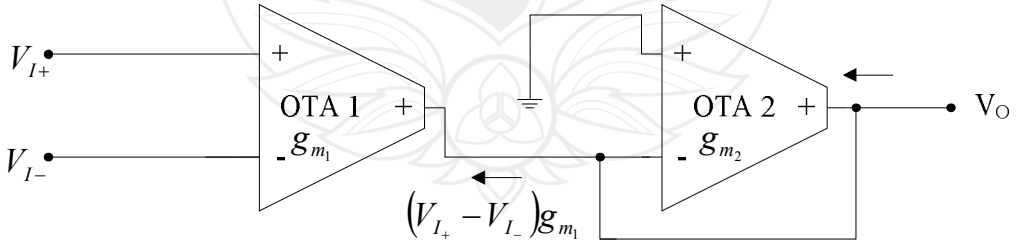


Figure 3.7 A Schematic of Power Combined Active BALUN Using OTA

The nodal analysis is taken at the output of OTA 1 which gives:

$$\left(V_{I_+} - V_{I_-}\right)g_{m_1} - V_O g_{m_2} = 0 \tag{20}$$

Therefore

$$V_O = \left(V_{I_+} - V_{I_-}\right)\frac{g_{m_1}}{g_{m_2}} \tag{21}$$

To make the input and output power equal, the following criteria must be met.

$$g_{m_2} = g_{m_1} \tag{22}$$

Therefore, a single ended output power is the same as the differential input power

$$V_O \cong \left(V_{I_+} - V_{I_-}\right) \tag{23}$$

Or by taking an equivalent model

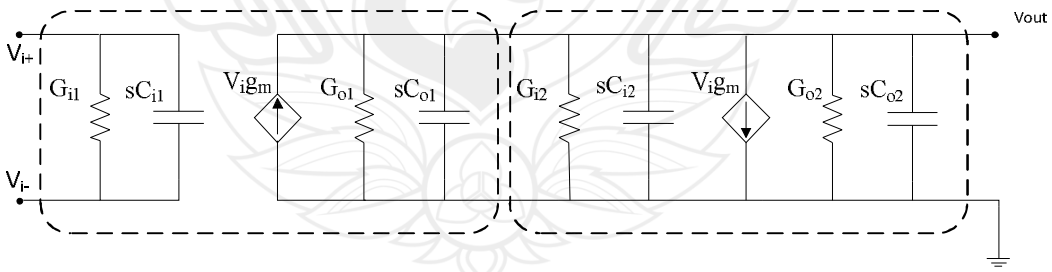


Figure 3.8 An Equivalent Model of Power Combined Active BALUN

To calculate input impedance by an equivalent model to connect a voltage source to input and connect an output to ground.

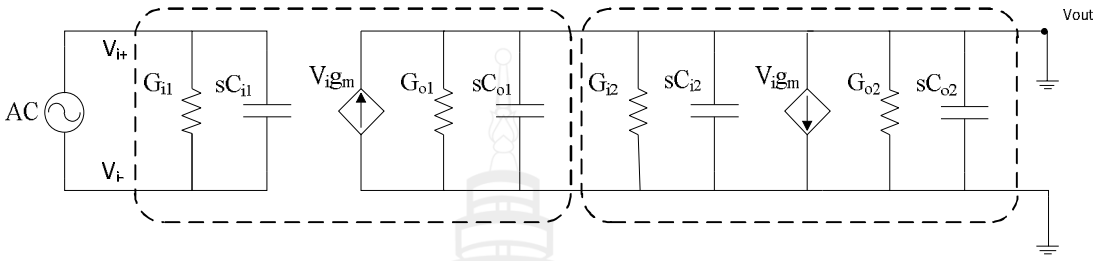


Figure 3.9 An Equivalent Schematic Used to Calculate Impedance of an Input of Power Combined Active BALUN

Reduced to

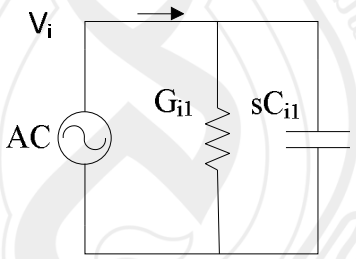


Figure 3.10 An Equivalent Schematic Used to Calculate Impedance of an Input of Power Combined Active BALUN (Reduced)

To calculate I_i assume that

$$I_i = V_i\left(G_i + sC_i\right) \tag{24}$$

Then input impedance is equal to

$$Z_{in} = \frac{V_i}{I_i} = \frac{1}{G_i + sC_i} \tag{25}$$

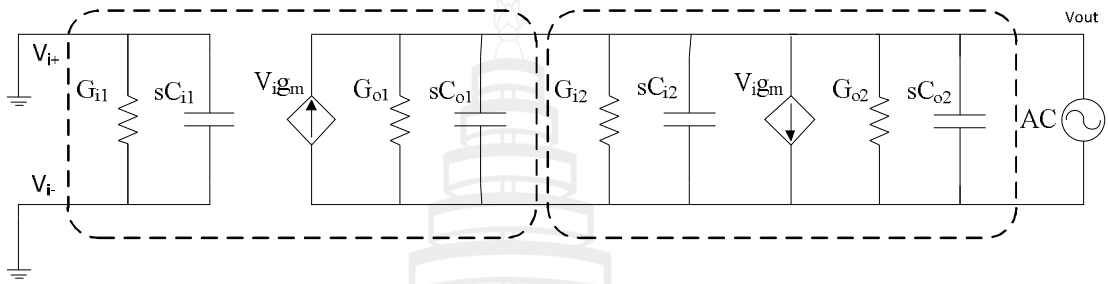


Figure 3.11 An Equivalent Schematic Used to Calculate Impedance of an Output of Power Combined Active BALUN

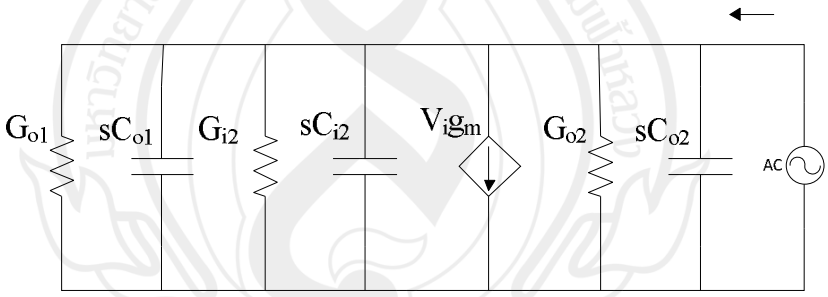


Figure 3.12 An Equivalent Schematic Used to Calculate Impedance of an Output of Power Combined Active BALUN (Reduced)

Then I is equal to

$$I_i = V_i\left(g_{m_2} + G_{i_2} + G_{0_1} + G_{0_2} + s\left(C_{i_2} + C_{o_1} + C_{o_2}\right)\right) \tag{26}$$

So output impedance should be

$$Z_{out} = \frac{1}{\left(g_{m_2} + G_{i_2} + G_{0_1} + G_{0_2} + s\left(C_{i_2} + C_{o_1} + C_{o_2}\right)\right)} \tag{27}$$

Or assume that $G_{i_3} + G_{o_1} + G_{o_3}$ are near to zero when compared g_{m_2} to

$$Z_{out} \cong \frac{1}{\left(g_{m_2} + s\left(C_{i_2} + C_{o_1} + C_{o_2}\right)\right)} \tag{28}$$

Then the output voltage in each side can be calculated in the equivalent cuicuit

$$V_o = \frac{\left(V_{I^+} - V_{I^-}\right)\left(g_m + G_{I_1} + G_{I_2} + s\left(C_{I_1}\right)\right)}{g_{m_2} + G_{O_1} + G_{O_2} + s\left(C_{I_2} + C_{O_1} + C_{O_2}\right)} \tag{29}$$

CHAPTER 4

SIMULATION RESULTS

4.1 Simulation Tool and Method

To verify the validity of the proposed BALUN, the transient, frequency response of signal splitters, transconductance and Z impedance was simulated by HSPICE 2007.3 with two environments 0.35 μm SiGe BiCMOS model and 90 nm IBM 9RF-CMOS process.

4.1.1 Experimental Environment

Simulator

HSPICE® is the industry's most popular simulator for accurate circuit simulation and offers foundrycertified MOS device models with state-of-the-art simulation and analysis algorithms. Analog/RF/mixed-signal IC design, cell and memory characterization, and chip/package/board/backplane signal integrity simulation are also widely used. In this research, HSPICE ® on version 2003.7 is used. SPICE stands for Simulation Program with Integrated Circuit Emphasis. It is the predominant tool used to simulate circuits, and was developed at UC Berkeley in the 1970s."H" in HSPICE means to be commercialized by Shawn and Kim Hailey of Meta Software. To analyze a circuit and plot the results of an analysis with a tool called Avanwaves.

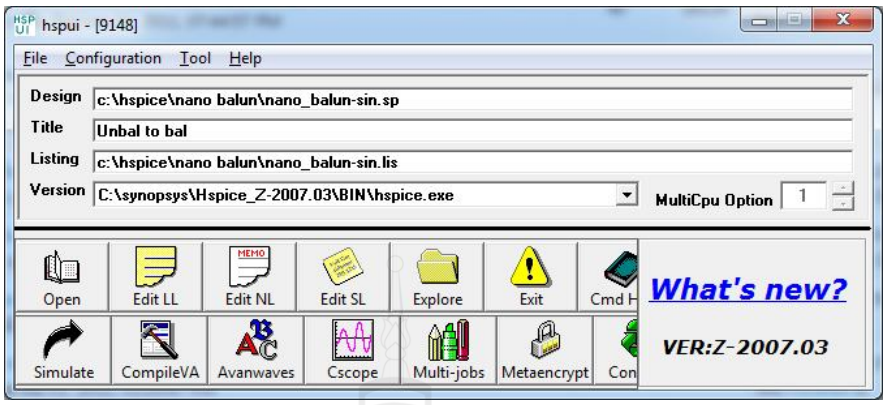


Figure 4.1 HSPICE

4.2 CMOS Model

4.2.1 AMS 0.35 µm SiGe BiCMOS

For this simulation, 0.35 µm SiGe BiCMOS design kit provided by the Austria Microsystems was used and this fabricated model was used for HSPICE simulator. The 0.35µm SiGe BiCMOS process is based on 0.35µm mixed-signal CMOS process (Kelly, Power, Oapos & Neill, 2003) with low noise MOS transistors .In this thesis, an AMS S35D4M5SiGe Bi-CMOS was used as a fabricated model, and another option of CMOS I/O transistors voltage is 3.3/5V.

Table 4.1 An Overview of AMS S35D4M5 SiGe Bi-CMOS Technology

Process Technology Specifications	Units	S35D4M5
Drawn MOS Channel Length	µm	0.35
Drawn Emitter Width	µm	0.4
Operating Voltage CMOS	V	3.3 and 5V
Number of Metal Layers	#	4

Table 4.1 (Continued)

Process Technology Specifications	Units	S35D4M5
Number of Poly Layers	#	4
Substrate Type		p
Diffusion Pitch	µm	0.9
Metal1/2/3 Pitch	µm	0.95/1.1/1.2
Poly1 Pitch	µm	0.8
Thick Metal 4 pitch	µm	-
High Resistive Poly	kOhm/#	-
Poly1 / Poly2 Precision Caps	fF/µm²	0.9
Metal 2 / Metal 3 Precision Caps	fF/µm²	1.25
N/PMOS Active Channel Length	µm	0.30/0.30
N/PMOS Saturation Current	µA/µm	540/240
Gain	-	160
Early Voltage VAF	V	100
HS-HBT: BVceo	V	2.7
ft / fmax	GHz	60 70

From **Euro Practice-IC.** (2012). Retieved August 18, 2012, from http://www.europractice-ic.com/technologies_AMS.php?tech_id=SiGe

4.2.2 IBM 90 nm RF CMOS

On IBM 90 nm CMOS process which has 9SF, 9LP and 9RF due to different applications in this research, 9RF fabricated model for HSPICE simulatoris used by MOSIS. The 90 nm CMOS containing 5-10 metal layers (Bohr, 2002). low voltage and using copper as metallization with low-k dielectric technologymakes this process ideally suitable for a wide range of high performance RF applications up to 140 GHz of ft.

Table 4.2 The 90 nm of an IBM 9RF CMOS

Feature	Unit	9RF
Process Generation	(nm)	90
Lpoly	(nm)	63
Vdd	(V)	1.0/1.2
I/O Voltage Options	(V)	1.8/2.5/3.3 tol
Std SRAM cell	(μm^2)	1.21
Dense SRAM cell	(μm^2)	.99
Levels of Metal	#	5-10
Metallization		Cu
Dielectric	(ILD)	Low-k
Power	(uW/MHz/gate)	0.006
Density	(Kgates/mm2)	400
MIMCap.	(fF/um2)	1.0
Varactor		Mos
Analog thick metal		yes

From Mecke, J. (2004). IBM Foundry Offeringsoundry Offerings. Retrieved August 21, 2012, form http://www.gobookee.com/get_book.php?u=aHR0cDovL3cyLmNhZGVuY2UuY29tL3doaXRlcGFwZXJzL3dpcmVsZXNzX3NvbHV0aW9uc19zYW5kaWVnb18wMTA2MDUucGRmCklCTSBGb3VuZHJ5IE9mZmVyaW5ncyAtIENhZGVuY2UgRGVzaWduIFN5c3RlbXM=

4.3 Tranconductance Versus Current Bias

To show that transconductance (g_m) of an OTA can be adjusted by changingcurrent bias (I_B). In this simulation, 0.35 μm SiGe BiCMOS and 90 nm 9RF CMOS is biased by the same current of 50 μA, 100 μA, 150 μA and 200 μA., and voltage input in AC analysis is 1 V. The result is shown inthe figure below.

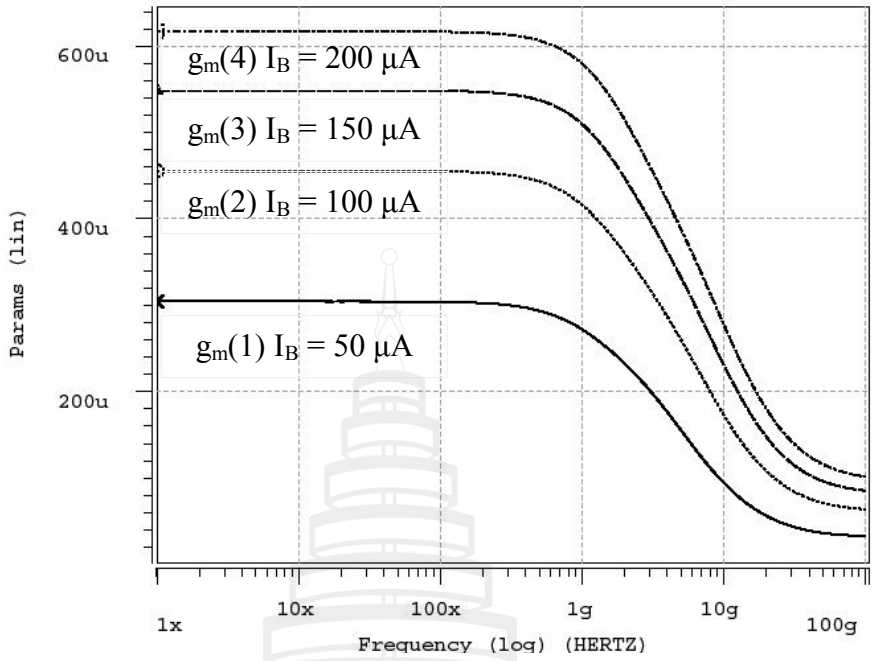


Figure 4.2 A Transconductance (g_m) Related to I_B bias of 0.35 µm Si-GeBiCMOS

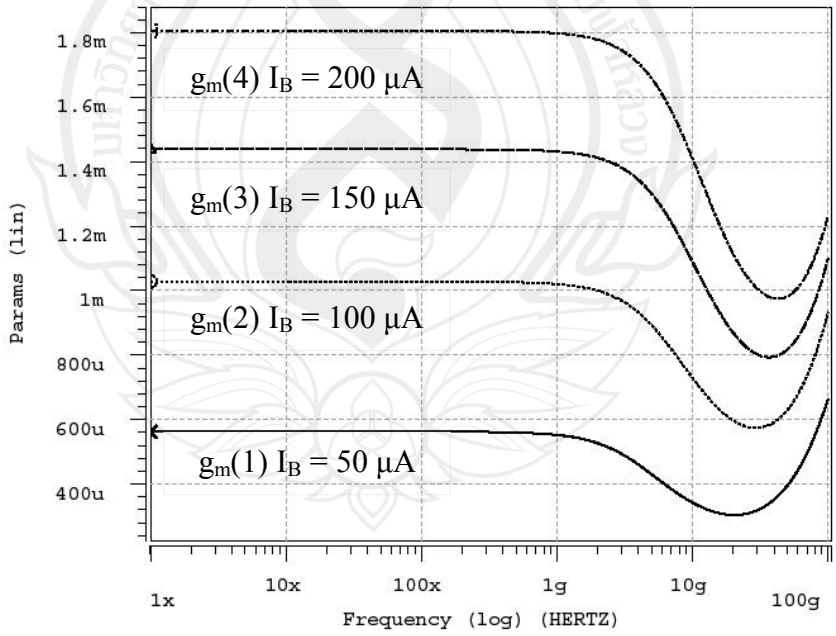


Figure 4.3 A Transconductance (g_m) Related to I_B bias Based on IBM 9RF 90nm CMOS

4.4 Power Split BALUN Results

4.4.1 Results from 0.35 µm SiGe Bi-CMOS Power Split BALUN

The output magnitudes are shown in Figures 4.4, 4.6 and 4.8; then Figures 4.5, 4.7 and 4.9 shows the differential signals between output and input. For AMS 0.35 Si-GeBiCMOS simulation, a small sine wave signal input of 10 mV PP at 10 MHz is used and the current bias of OTA 1 and OTA2 are 75 µA. The tunable current of OTA 3 and OTA 4 are in steps of 100 µA, 200 µA and 300 µA to show the tunable output magnitude.

The results of the different frequency ranges and phase imbalances are shown in Figure 4.4 and Figure 4.5 which the current bias of OTA 1 and OTA 2 are 75 µA and the current bias of OTA 3 and OTA 4 are 300 µA.

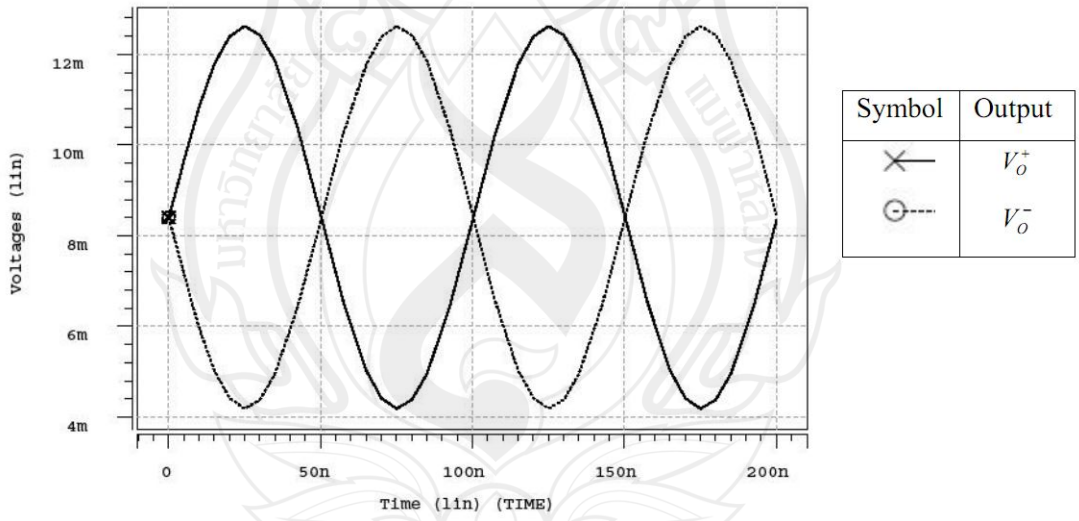


Figure 4.4 Result of 100 µA Current Bias for OTA 3 and OTA 4 with Output from V_O^+ and V_O^-

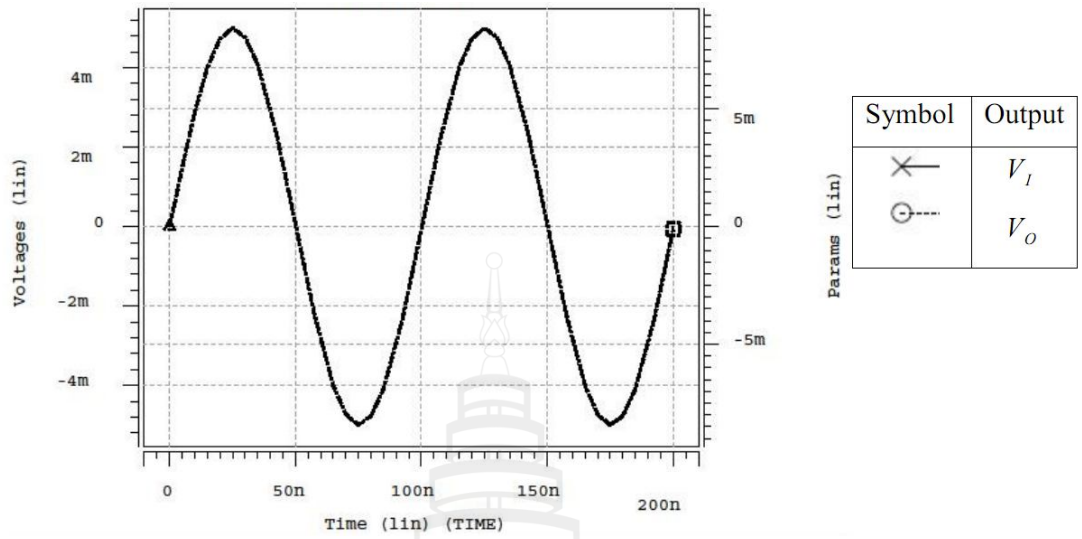


Figure 4.5 Result of 100 µA Current Bias for OTA 3 and OTA 4 with Voltage Output from Differential Output Compared to Input

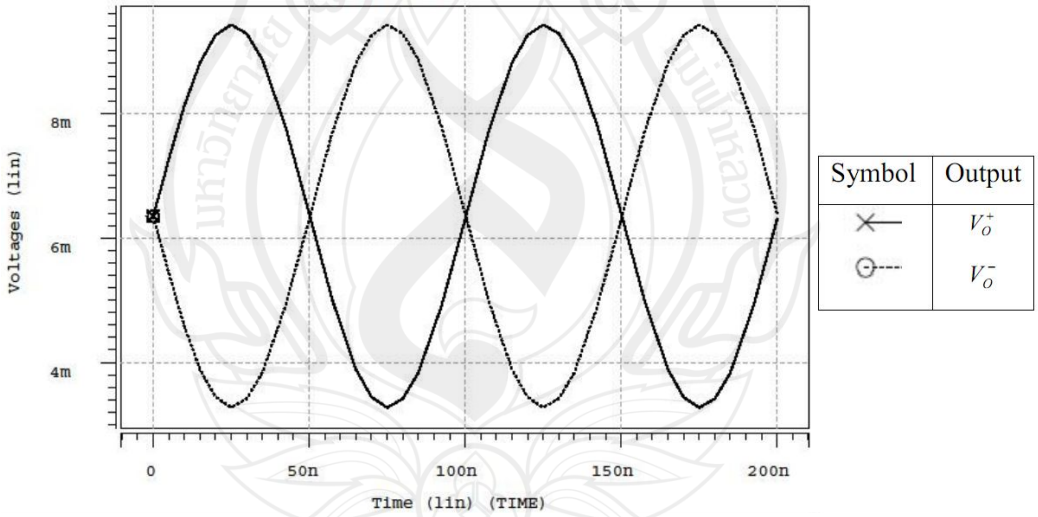


Figure 4.6 Result of 200 µA Current Bias for OTA 3 and OTA 4 with Output from V_O^+ and V_O^-

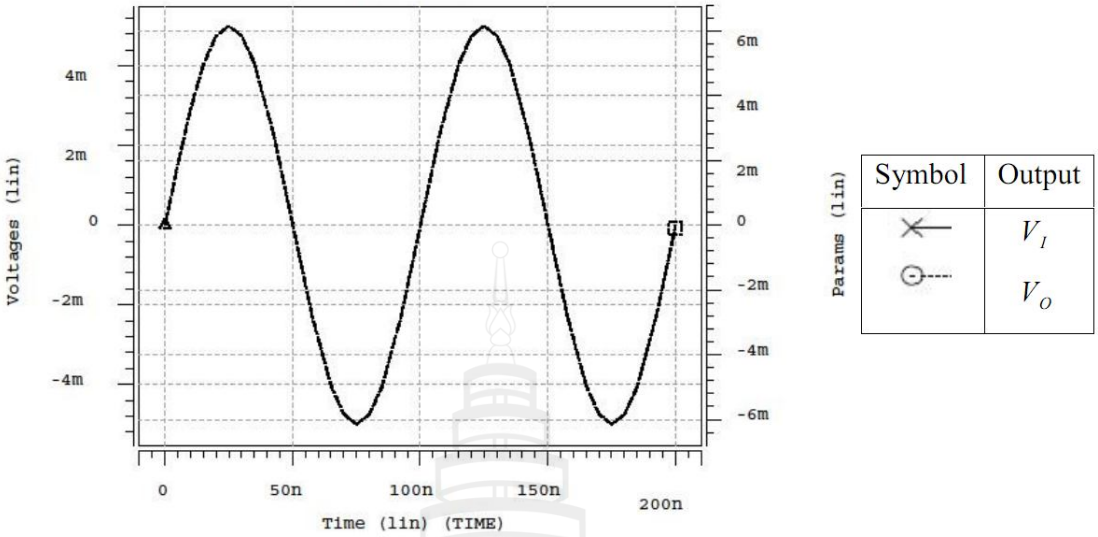


Figure 4.7 Result of 200 µA Current Bias for OTA 3 and OTA 4 with Output Voltage from Differential Output Compared to Input

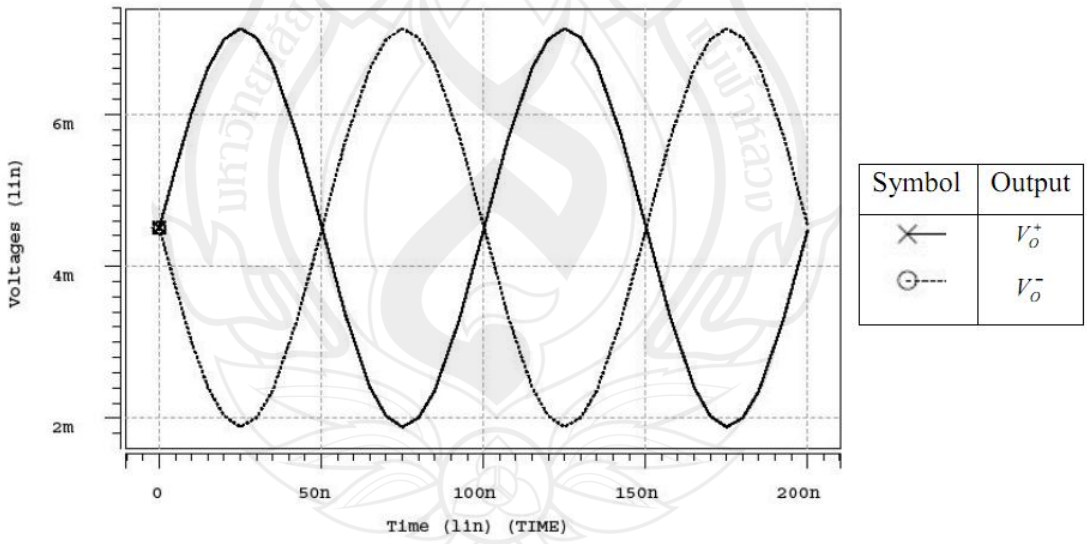


Figure 4.8 Result of 300 µA Current Bias for OTA 3 and OTA 4 with Output from V_O^+ and V_O^-

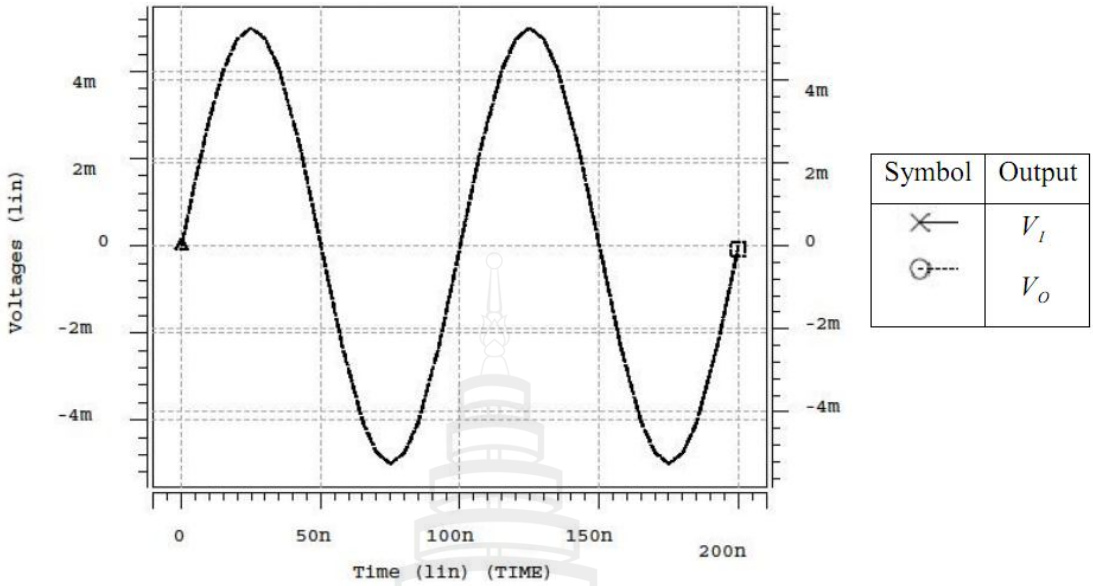


Figure 4.9 Result of 300 µA Current Bias for OTA 3 and OTA 4 with Output Voltage from Differential Output Compared to Input

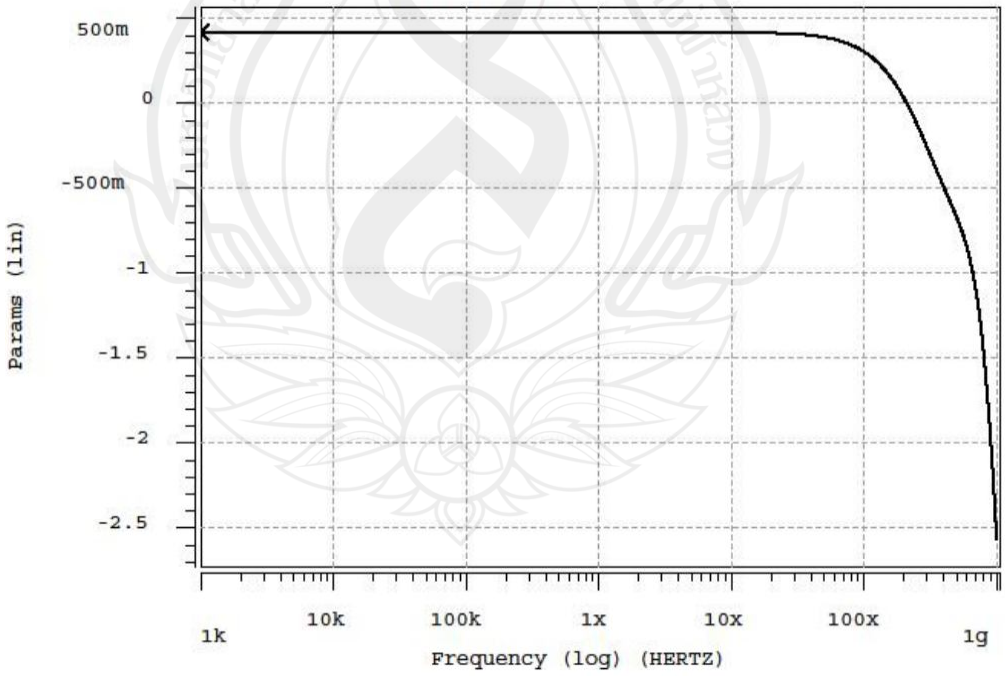


Figure 4.10 Result of 300 µA Current Bias for OTA 3 and OTA 4 with Voltage Differential Output in 1 GHz Frequencies Range in dB

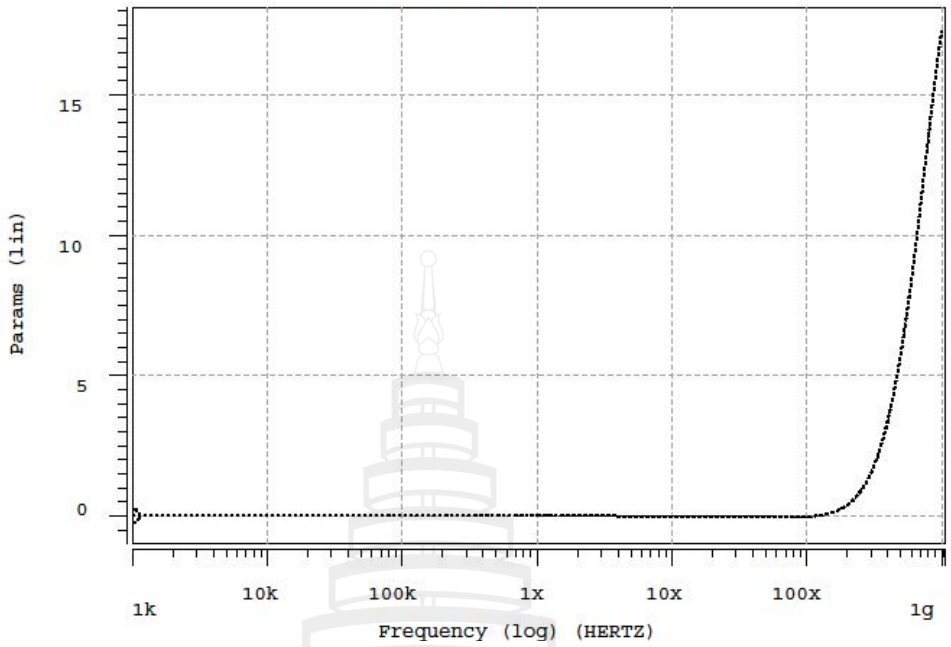


Figure 4.11 Result of 300 µA Current Bias for OTA 3 and OTA 4 with Phase Imbalance of Differential Output

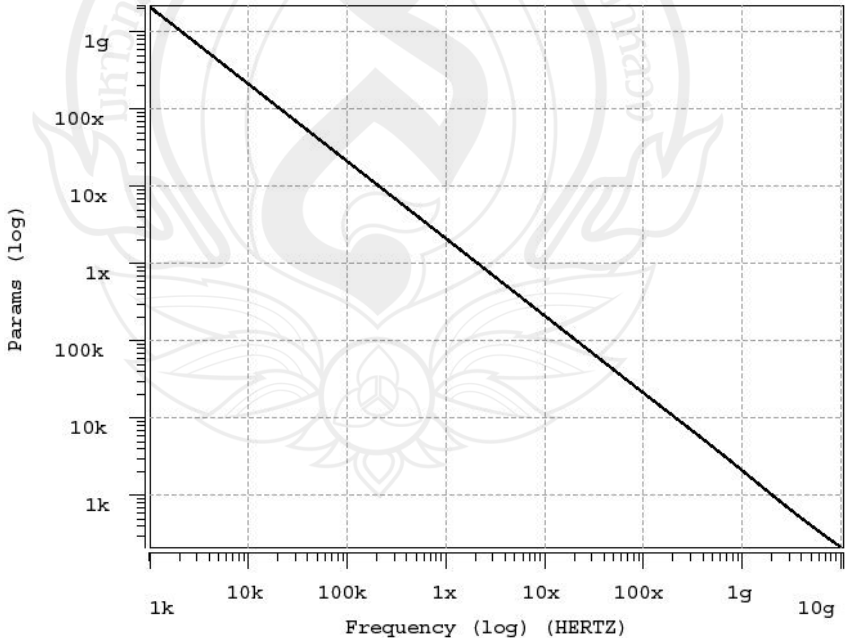


Figure 4.12 Frequencies Response of Input Impedance Power Split BALUN in Ohm Versus Frequencies

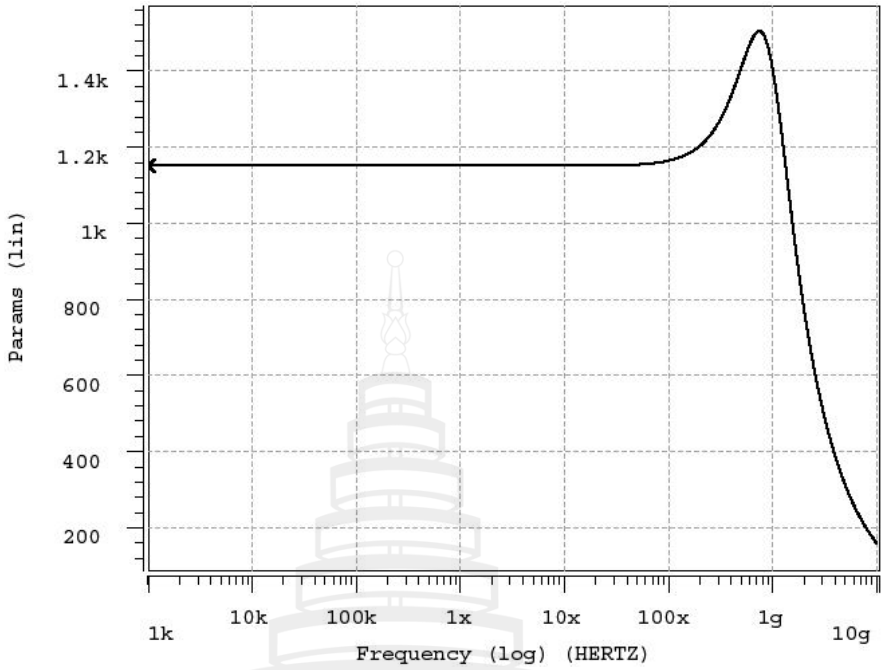


Figure 4.13 Frequencies Response of Positive Output Impedance Power Split BALUN in Ohm Versus Frequencies

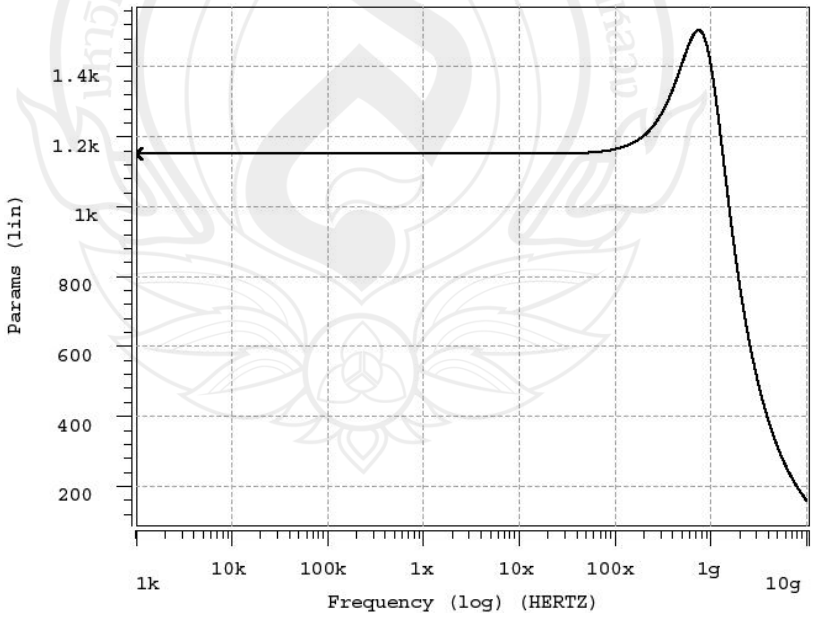


Figure 4.14 Frequencies Response of Negative Output Impedance Power Split BALUN in Ohm Versus Frequencies

4.4.2 Results from IBM 9RF CMOS Power Split BALUN

To verify the validity of the 90 nm RF CMOS BALUN based on the 90 nm IBM RF-CMOS process extracted by the MOSIS. For power split BALUN, the bias currents are 80 μA for OTA 1 and 2, and 172 μA for OTA 3 and 4. The frequencies responses are shown in Figure 4.15. Phase imbalance is shown in Figure 4.16. The transient response from 2.5GHz 10mV PP input is plotted in Figure 4.17, and z-impedance is shown in Figure 4.18, 4.19, and 4.20.

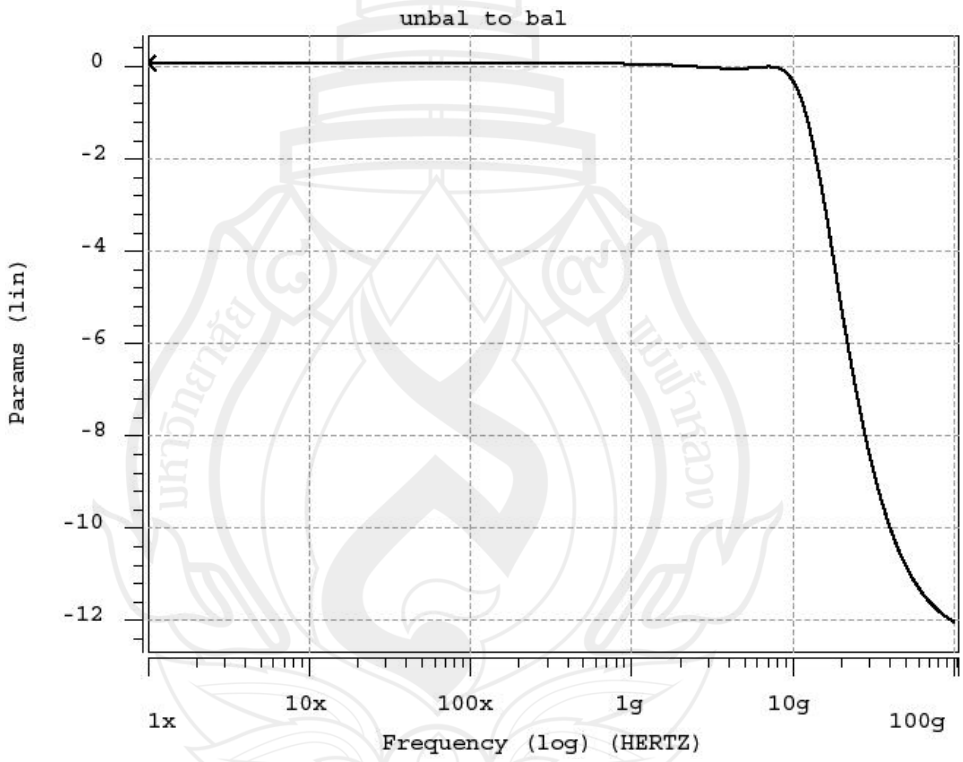


Figure 4.15 Frequencies Response and dB from V_o Output of Power Split BALUN, -3dB Bandwidth is15.7GHz

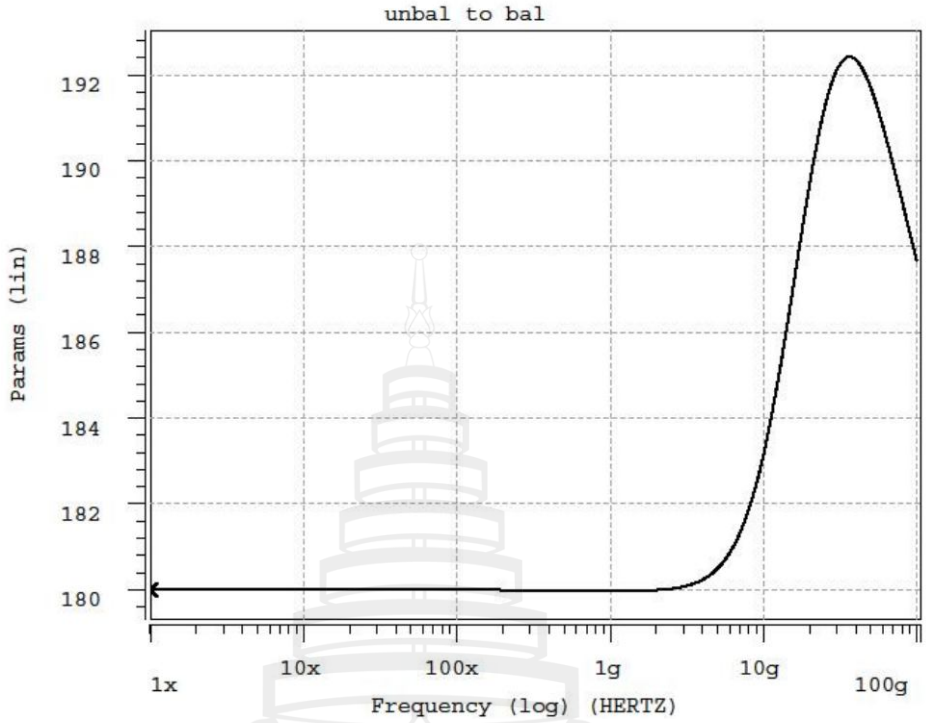


Figure 4.16 Frequencies Response of Phase Differential 180 Degree Output from Power Split BALUN with 7.14º of Phase Imbalance at -3dB (15.7GHz)

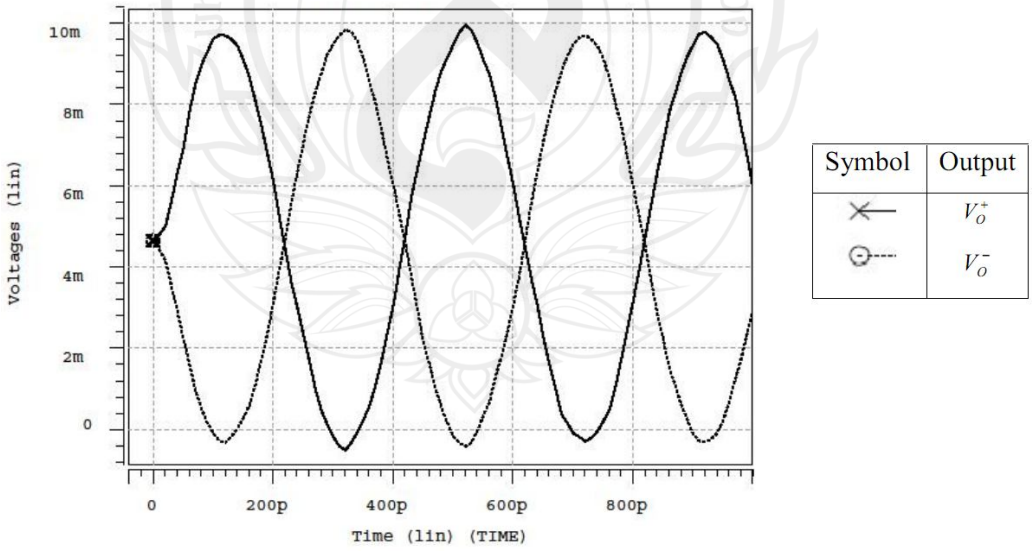


Figure 4.17 Drifferential Output of Power Split BALUN Transient Analysis for Input 10mV at 2.5GHz

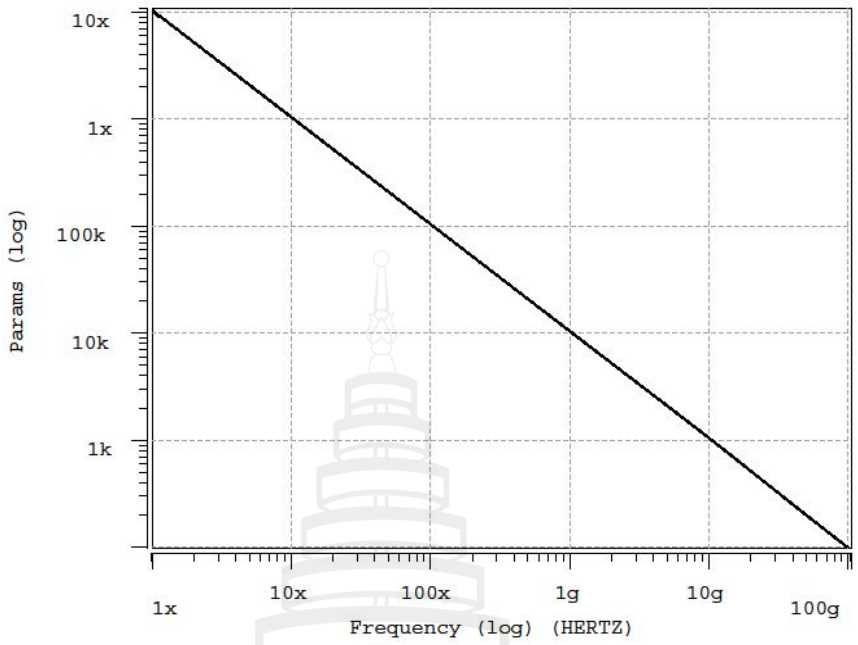


Figure 4.18 Frequencies Response of Input Impedance from Power Split BALUN

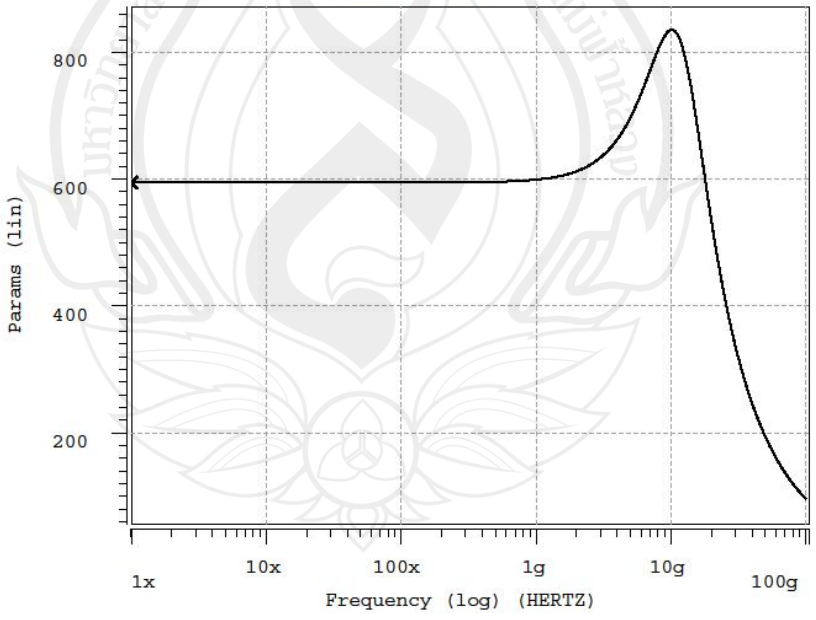


Figure 4.19 Frequencies Response of Positive Output Impedance from Power Split BALUN

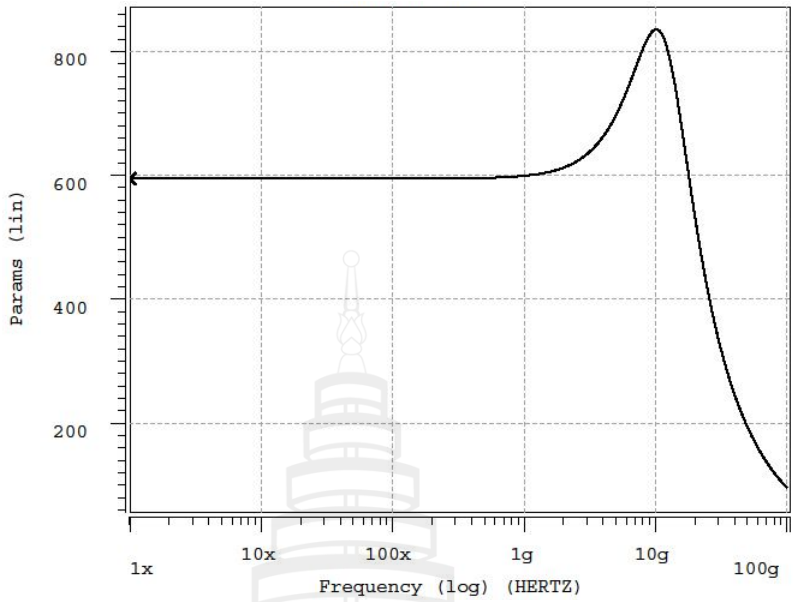


Figure 4.20 Frequencies Response of Negative Output Impedance from Power Split BALUN

4.5 Power Combined BALUN Results

4.5.1 Results from 0.35µm SiGe BiCMOS Power Combined BALUN

The output of the power combined BALUN is also simulated with the same simulator and MOSFET model. The biases current are 190 µA for both OTAs. The output frequency response is shown in Figure 4.21, and the transient response based on two 10MHz 50mV PP out phase inputs is shown in Figure 4.22.

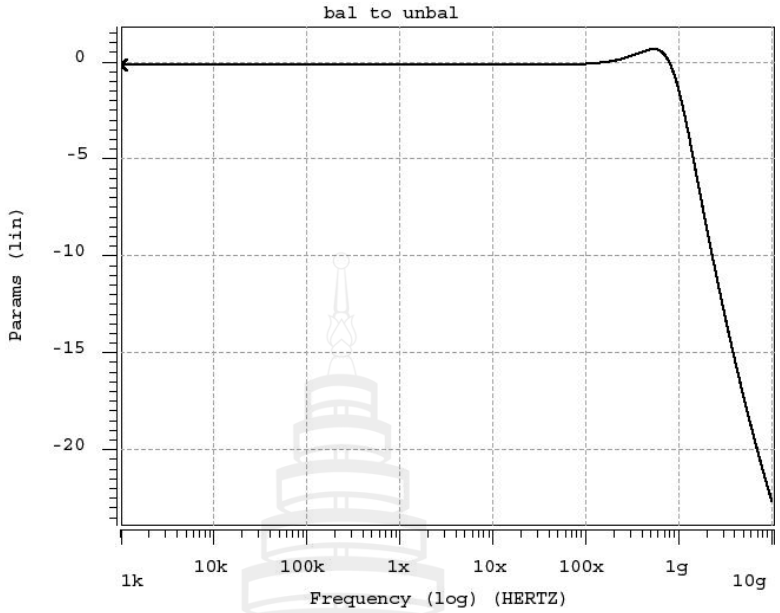


Figure 4.21 Frequencies Response and dB from V_o Output of Power Combined BALUN, -3dB Bandwidth is 1.19 GHz

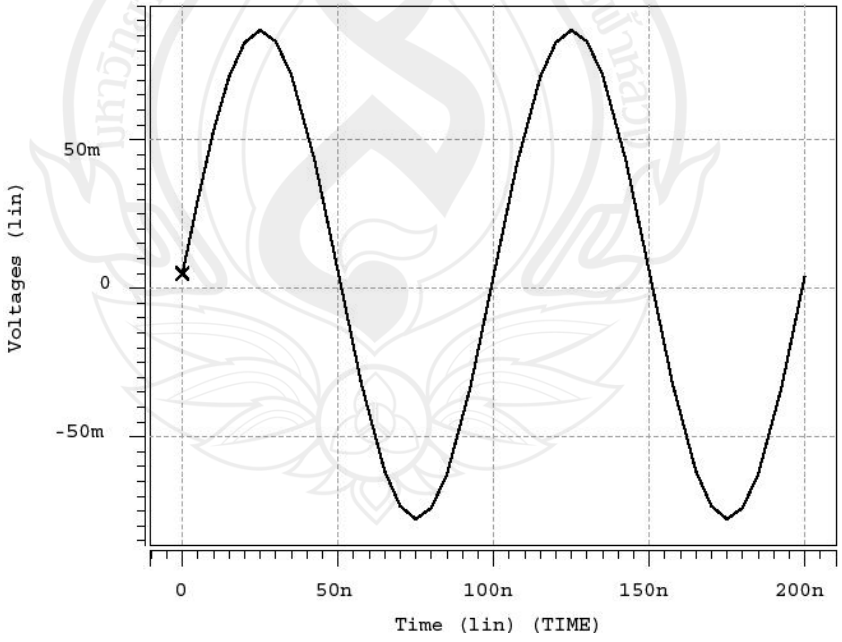


Figure 4.22 A Transient Analysis of Combined Output of Power Combined BALUN for 2 Input of 50mV PP which 180º Out Phase at 10 MHz

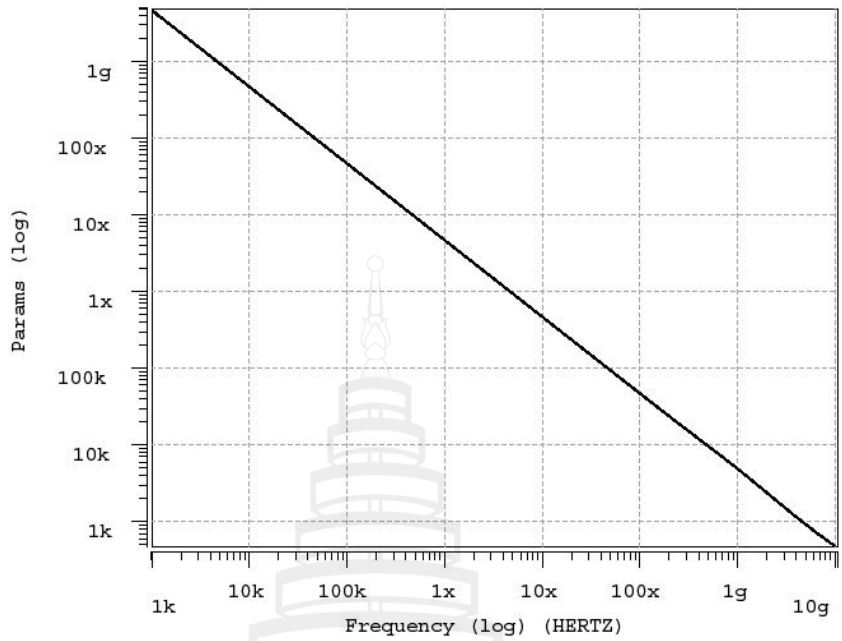


Figure 4.23 Frequencies Response of Positive Input Impedance from Power Combined BALUN

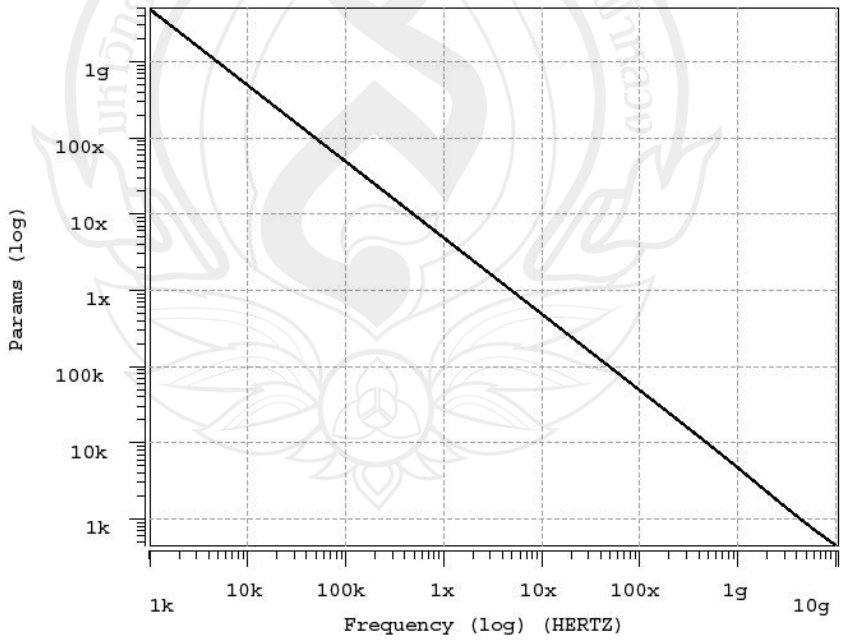


Figure 4.24 Frequencies Response of Negative Input Impedance from Power Combined BALUN

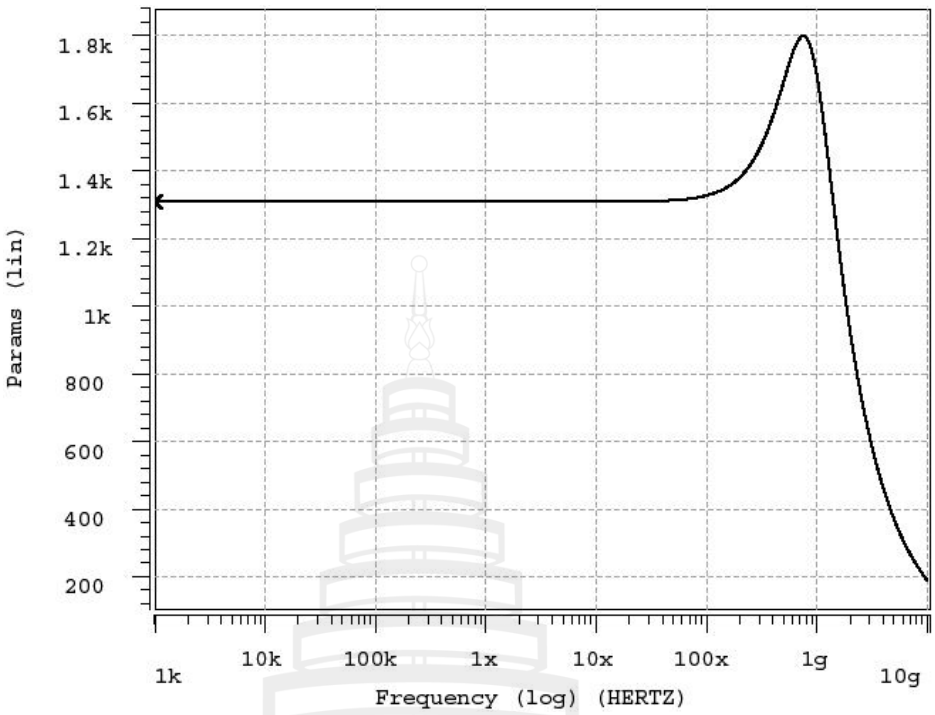


Figure 4.25 Frequencies Response of Output Impedance from Power Combined BALUN

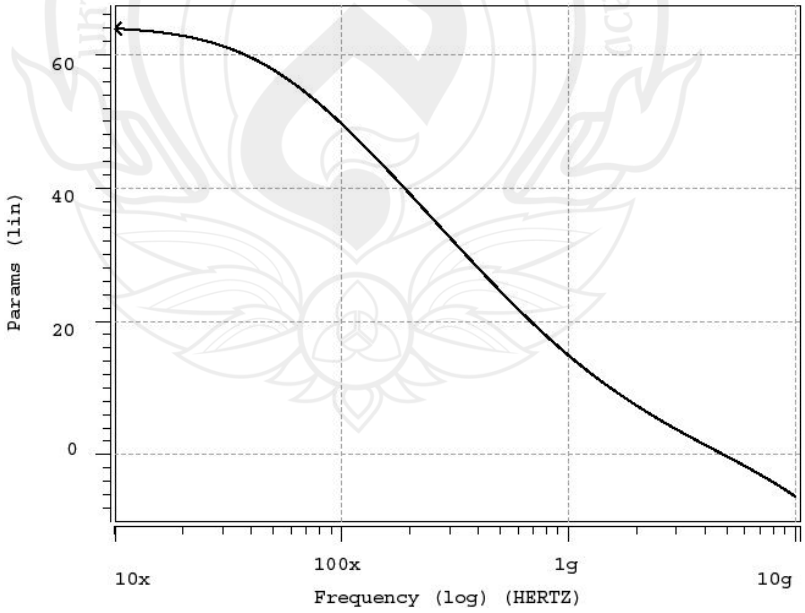


Figure 4.26 CMRR Frequencies Response of Power Combined BALUN

4.5.2 Results from IBM 9RF CMOSPower Combined BALUN

The output of the powercombined BALUN is also simulated with the same simulator and MOSFET model as the power split BALUN. The biases current are 190 μA for both OTAs. The output frequency response is shown in Figure 4.27 and the transient response based on two 2.5GHz 10mV PP out phase inputs is shown in Figure 4.28, and z-impedance of all input and output portsis showninFigure 4.29, 4.30 and 4.31.

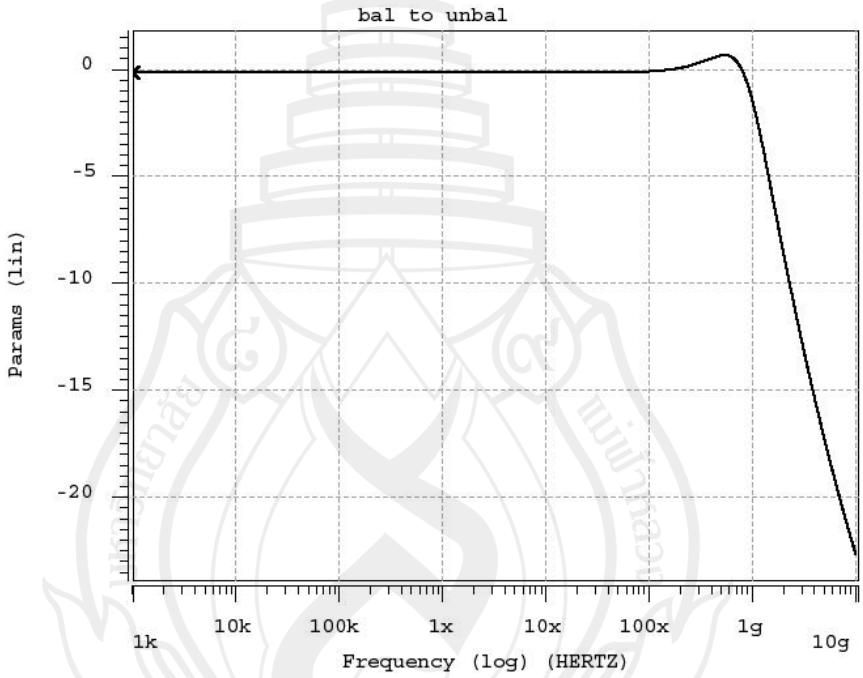


Figure 4.27 Frequencies Response and dB from V_o Output of Power Combined BALUN, -3dB Bandwidth is 17.5 GHz

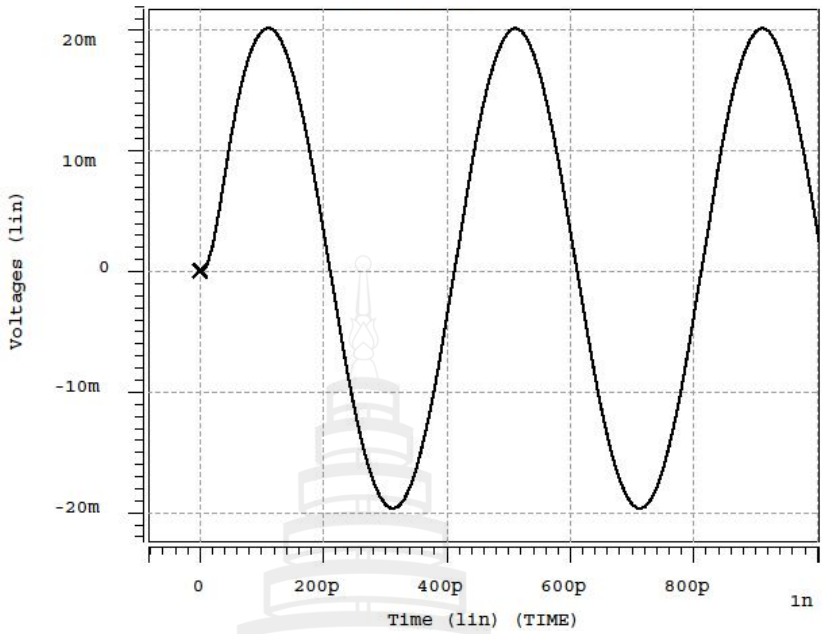


Figure 4.28 A Transient Analysis of Combined Output of Power Combined BALUN for 2 Inputs of 10mV PP which 180º Out Phase at 2.5GHz

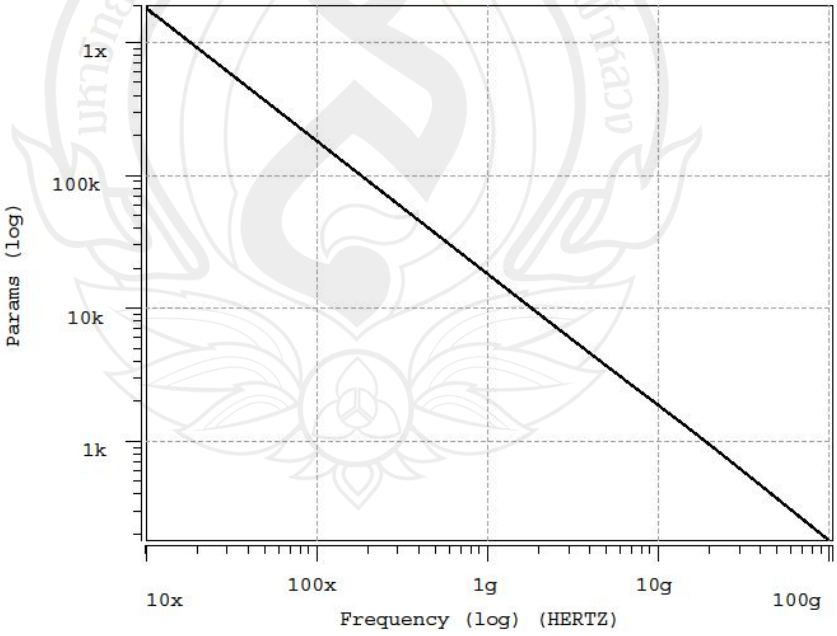


Figure 4.29 Frequencies Response of Z Impedance from Power Combined BALUN Positive Input

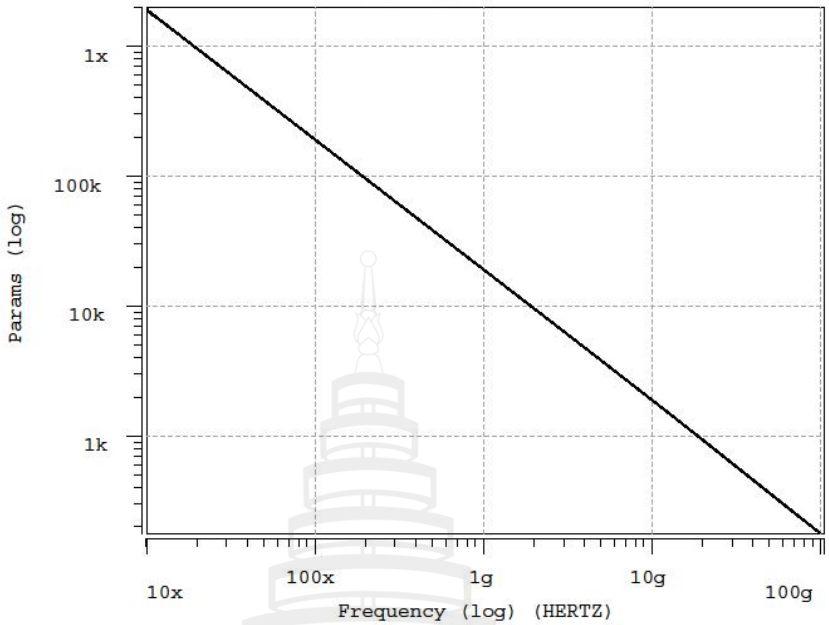


Figure 4.30 Frequencies Response of Z Impedance from Power Combined BALUN Negative Input

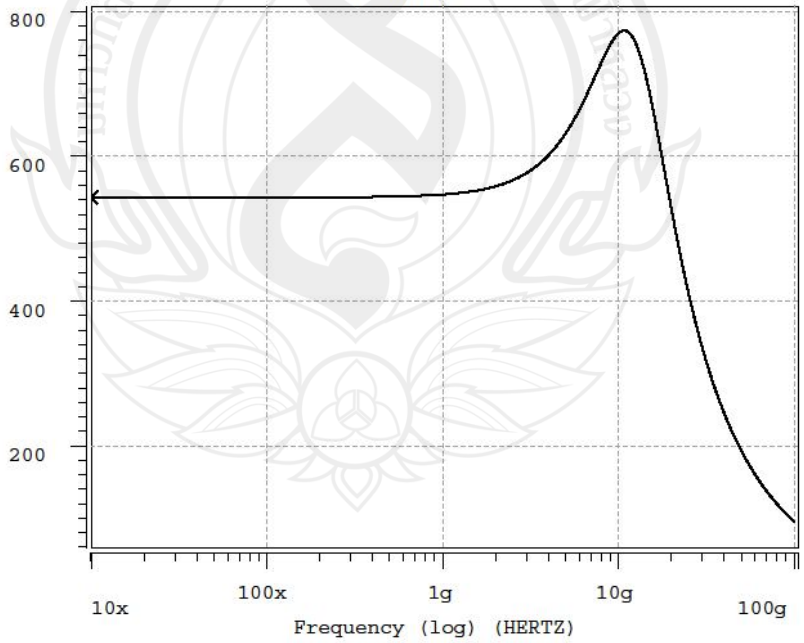


Figure 4.31 Frequencies Response of Z Impedance from Power Combined BALUN Output

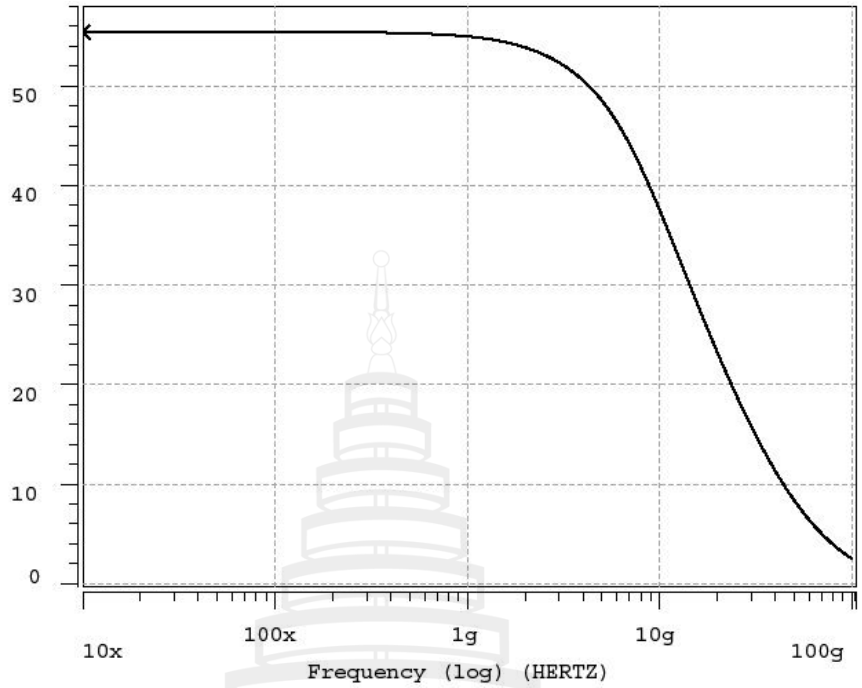


Figure 4.32 Frequencies Response of Power Combined BALUN CMRR

Table 4.3 Compared Current Bias vs gm and Vdd, Vss between 0.35µm Si-Ge Bi-CMOS and 90 nm IBM 9RF CMOS process

Process		**0.35um Si-Ge Bi-CMOS**	**90nm IBM 9RF CMOS**
Current bias	50 µA	300µS	540µS
	100 µA	460µS	1.04 mS
	150 µA	540µS	1.44 mS
	200 µA	620µS	1.8 mS
Vdd		3.3V	0.5V
Vss		-3.3V	-0.5V

From Table 4.3, comparing the transcoductance in OTA from0.35µm SiGe BiCMOS and IBM 9RF CMOS with the same reference current bias as 50 µA, 100 µA, 150 µA and 200 µA is noted. The 50 µA current in 0.35µm Si-Ge Bi-CMOS that

gives 300 μS of the transconductanceand the IBM 9RF CMOS that givesup to 450 μS have almost been compared twice. When the current bias increases to 100 μA, the model of 0.35μm SiGe BiCMOS will give the transconductanceto 460 mS, and 1.04 mS for the model of IBM 9RF CMOS. When the current bias increases to 150μA and 200μA, the transconductance of the 0.35μm SiGe BiCMOS increases to 540 μS and 620 μS respectively and the IBM 9RF CMOS modelincreases two times to 1.44 mS and 1.80 mS, but these two models still use Vdd and Vss at the same rate which is 3.3 V and-3.3 V for the 0.35μm Si-Ge Bi-CMOS, and 0.5 V and-0.5 V for the IBM 9RF CMOS.

Table 4.4 Compared BALUN Performance between 0.35μm SiGe BiCMOS and 90 nm IBM 9RF CMOS

Process	**0.35μm Si-Ge Bi-CMOS**		**90nm IBM 9RF CMOS**	
Type of BALUN	Power Split	Power Combined	Power Split	Power Combined
Number of Transistor	16	8	16	8
Bandwidth	-3dB @ 1GHz	-3dB @ 1.19 GHz	0-15.7 GHz	0- 17.5 GHz
Phase imbalance	0.02 º at 100 MHz	-	7.14º at 15.7 GHz	-
Z input	>2 GΩ @ DC	>4 GΩ @ DC >4 GΩ @ DC	>10MΩ @ DC	>2 MΩ @ DC >2 MΩ @ DC
Z output	1.16 kΩ between 0- 100 MHz 1.16 kΩ between 0- 100 MHz	1.12 kΩ between 0-100 MHz	600 Ω between 0-1 GHz 600 Ω between 0-1 GHz	540 Ω between 0- 1 GHz
CMRR	-	50 dB between 0- 100 MHz	-	50 dB between 0- 4 GHz

Table 4.4 for the power split and power combined baluns begins with the bandwidth of the power split balun of0.35μm Si-Ge Bi-CMOS which is 1 GHz at point- 3 dB and the power combinedbalun which is 1.19 GHz. But for IBM 9RF

CMOS- 3 dB, the bandwidth of the power split balun is 15.7 GHz and the power combined balun is 17.5 GHz, which is several times higher than the 0.35μm SiGe BiCMOS. The Z input impedance of the power split balun is greater than 2 GΩ and the power combined balun isgreater than 4 GΩ. But for the IBM 9RF CMOS, the power split balun is greater than 10 MΩ and the power combined positive and negative input is greater than 2 MΩ. The Z output power split model of the 0.35μm SiGe BiCMOS is greater than 1.16 kΩ in the range of 0-100 MHz and the power combined model is greater than 1.12 kΩ in the same frequency.For the IBM 9RF CMOS, the power split balun in the frequency range of 0-1 GHz is 600 Ω and the power combined balun is 540 Ω.For the phase imbalance of the 0.35μm Si-Ge Bi-CMOS, the power split balun will be not more than 0.02 degrees at 100 MHz and CMRR up to 50 dB in the same frequency range, but in the case that 90 nm is 15.7 GHz and the imbalance does not exceed 14.7º and the power combinedCMRR with a 90 nm to 50 dB is in the 0-4 GHz.

CHAPTER 5

CONCLUSION

Previously, the passive BALUN such as the transformer BALUN, the wavelength BALUN and RLC BALUN needed large space which varied inversely with frequency and wasdifficult to be tuned or fabricated within system on chip. After active BALUN circuits with a single transistor or differential pair transistor have come, they can decrease the size of the circuit and are easier to be adjusted to fit the required frequency.

However, there are still some limitations to how each type of transistors works based on its characteristics and quality, including passive sessions in the circuit, because it cannot be used in high-frequency range or wide bandwidth. In order to develop the integrated circuit BALUN, a CCCII module is used as its characteristics can make the BALUN used in wider frequency and the impedance adjusted to fit the required frequency. However, the CCCII structure is complicated because there are various types of the transistors. This causes the fabricated procedure on the Bi-CMOS to be more expensive and larger size than the active OTA BALUN. The design based on the OTA simple structure decreases the number of the transistors and reduces the size of the circuit while increasing response frequencies when fabricated on the same model. Thus, this less complicated OTA BALUN should be inexpensive to be fabricated into system on chip. Its performance is summarized below.

5.1 Results of the Simulation

5.1.1 The results of the simulationapparently showed thatthe limitations of the OTA BALUN depend on the characteristics of the fabricated model. When

changing the model from 0.35µm SiGe BiCMOS to 90 nm 9RF CMOS, the frequency response is better with less pressure and higher reliability.

5.1.2 The simulation result of the frequency response of the power split BALUN in 0.35µm SiGe BiCMOS is in the range up to 1 GHz frequencies cutoff while, in 90 nm9RF CMOS,the range is up to 15.7 GHz and the phase imbalance is in the recognized level by using the same OTA but different model.

5.1.3 For the power combined BALUN, the frequency response is little different in the wider range of 1.19 GHz for the 0.35µm SiGe BiCMOS and 17.5 GHz for the 90 nm 9RF CMOS while the CMRR values of both models are higher than 50 dB in low frequency phase.

5.1.4 Both power combined and power split BALUNs can be used to adjust eachbias current in the OTA circuit to compensate for the output to fit the required result.

5.1.5 The input impedance of both power split and power combined BALUNs is very high, resulting from the characteristics of the MOS transistor model and the differential pair OTA. Thus, no current is transferred from the input directly to the output, which providesthe less reflected signal from the input and the regenerated signal to the output. As a result, the characteristics of the s-parameter cannot be directly used to describe a performance of this BALUN.

5.2 Limitations

5.2.1 The characteristics of the MOS transistor in each fabricated model have different bias currents and voltage limits, causing the limitationsof adjusting the bias current, as the BALUN is hardly to be tuned.

5.2.2 Another limitation of the OTA BALUN is frequency response on logarithm.The frequency is first shown in horizontal line response and slightly choking effect is shown in the high frequencies before reaching the cutoff frequencies point (-3dB) which makesthe response bandwidth unstable after that point. It is supposed that the effect came from the hidden inductance in each OTA module.

5.2.3 Compared with other BALUNs, the input and output impedance of this BALUN is many times higher (50 Ω and 75 Ω).Thus, this BALUN circuit needs to integrate the matching impedance circuit in order to make the impedance more suitable to be used with other communication circuits.

5.3 Future Work

5.3.1 Simulate more advanced models such as 65 nm IBM 10RFe CMOS for expanded frequency response.Decrease the size, test the fabricated model for use, and find environmental effectson the circuitsto reduce the limitations of the OTA BALUN circuit.

5.3.2 Improve the structure of the OTA module to increase frequency responses and integrate a part of the matching impedance to input and output.

5.3.3 Find solutions to explain the parasitic inductance that causes the choking effect before frequency cutoff (-3dB) in the OTA circuit in order to reduce the effects and make frequency response flat off before cutoff frequencies by using the Monte Carol analysis and the 3 dimensional fabricated simulation.

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APPENDICES

APPENDIX A

Austria Microsystem SiGe BiCMOS 0.35 μm

The concept of combining silicon (Si) and germanium (Ge) into an alloy for use in transistor engineering is an old one (Burghartz, Soyeur, Jenkins, 1996). However, because of difficulties in growing lattice-matched SiGe alloy on Si (Osamu, editor, 2007). this concept is reduced to practical reality only in the last 15 years. SiGe HBT (Cressler & Niu, 2003) technology was originally developed at IBM for the high-end computing market, that effort, however, failed to CMOS, primarily because of its high power consumption.

In the early 1990s, IBM refocused SiGe program for developing in communications market. Interestingly, for RF communications circuits, SiGe HBT consumes much less power than CMOS to achieve the same level of performance. Since then, significant progress has been made. SiGe technology is being developed and applied around the world, and then is in the product roadmap of every major telecommunication company. Applications range from wired and wireless communications circuits, to disk storages, to high speed high bandwidth instrumentation. The use of discrete SiGe HBTs and amplifiers in wireless devices is common place. Integrated SiGe chips can be found in GSM and CDMA wireless handsets and base stations, wireless LAN chipsets, and high-speed 10-40 Gb/s synchronous optical network (SONET) transceivers.

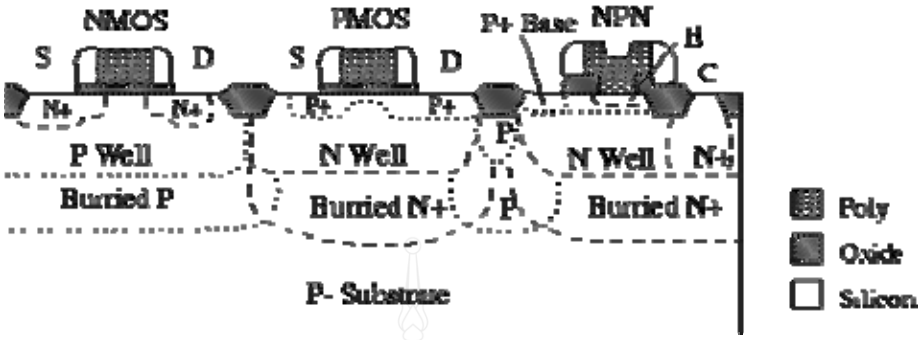

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Figure A1 Structure of NMOS, PMOS and Transistor on SiGe BiCMOS Process

Table A1 Characteristics of 0.35um SiGe BiCMOS

Process Name	unit	S35D3M2	S35D4M2	S35D4M5
Process Type	-	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS
Drawn MOS Channel	µm	0.35	0.35	0.35
Length, Drawn Emitter Width	µm	0.4	0.4	0.4
Operating Voltage CMOS	V	2.5-3.6	2.5-3.6	2.5-3.6 / 5.5
Number of Metal Layers	-	3	4	4
Number of Poly Layers	-	4	4	4
Substrate Type	-	P	P	P
Diffusion Pitch	µm	0.9	0.9	0.9
Metal1/2/3 Pitch	µm	0.95/1.1/1.2	0.95/1.1/1.2	0.95/1.1/1.2
Poly1 Pitch	µm	0.8	0.8	0.8
Thick Metal 4 pitch	µm	-	4.5	4.5
High Resistive Poly	kOhm/#	-	-	1.2
Poly1 / Poly2 Precision Caps	fF/µm²	0.9	0.9	0.9

Table A1 (Continued)

Process Name	unit	S35D3M2	S35D4M2	S35D4M5
Metal 2 / Metal 3 Precision Caps	fF/μm²	1.25	1.25	1.25
N/PMOS Active Channel Length	μm	0.3/0.3	0.3/0.3	0.3/0.3
N/PMOS Saturation Current	μA/μm	540/240	540/240	540/240
Gain	-	160	160	160
Early Voltage VAF	V	100	100	100
HS-HBT: BVceo	V	2.7	2.7	2.7
ft / fmax	GHz	60 / 70	60 / 70	60 / 70
HV-HBT: BVceo	V	-	-	5.5
ft / fmax	GHz	-	-	30 / 50

From TORKI, K. (2011). CMP. **In Workshop on Microelectronics beyond the GHz, Clermont-Ferrand.** Grenoble, France.

APPENDIX B

Tunable Active CMOS Balun Based on Operational Transconductance Amplifier

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***Abstract*—In modern communication systems, the signal splitter called BALUN (BALance to UNbalance) is required to interface a single ended device with a differential ended device. Most active BALUN use passive elements which cannot be tuned and require a large area on the integrated circuit. Though there is the controllable BALUN based on BiCMOS CCCII, the implemented circuit is quite large in transistor count and the cost of BiCMOS is very expensive. In this work, a new active BALUN based on CMOS OTA is proposed. By adjusting the transconductance of the composed OTAs, the characteristics of BALUN can be tuned electronically. Normally the size of the OTA is half of the size of the CCCII in transistor count. Therefore, the size of proposed structure is theoretically half of the CCCII counterpart. The design structure is simulated in the HSPICE based on the AMS 0.35µ CMOS process. Demonstrated in simulation results, the proposed structure can be a fair alternative in BALUN design due to adequate compatibility of BALUN characteristics such as power splitting and inverse phase.**

Keywords-component; Operational Transconductance Amplifier, Active BALUN, CMOS

I. INTRODUCTION

Nowadays, most transceivers are composed of both single ended (SE) and differential ended (DE) components. Therefore, a converter circuit called BALance to UNbalance (BALUN) converter is usually needed. Most BALUN designs are based on passive components [1], BJT [2], and BiCMOS[3]. Though these designs work well on their own, most transceivers are favored to be fabricated based only on complementary MOS (CMOS) to be placed among various digital functions. In addition, ability in tuning is also a good option in a BALUN [4, 7] to cover error in gain matching that is likely to occur with quite high probability in practical systems.

Interestingly, the operational transconductance amplifier (OTA) simulating voltage-controlled current source (VCCS) [5] is one of the favorite active analogue devices because the transconducatance can be tuned electronically via bias current. Therefore, key properties of its applications can be easily tuned via single or multiple bias currents. In addition, the OTA is usually small compared to the current controlled current conveyor (CCCII) which is formerly composed of a tunable active BALUN [4, 7]. In this paper, the novel active nanoscale CMOS BALUN is proposed based on OTAs. The proposed circuit will be easily placed in a mixed signal chip because it requires no passive elements and no different types of transistors.

II. THE BALUN

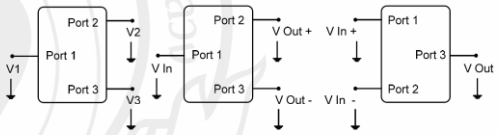

Figure 1. (a) BALUN (b) Signal Split BALUN (c) Signal Combine BALUN

A BALUN is a device for conversion between a single-ended signal and differential-ended signal structure as shown in Figure 1(a). For signal split BALUN, a differential signal can be considered as two signals from port 1 to port 2 and port 3 with equal voltage but 180 ° differential phases (Figure 1(b)). Another type is called signal combine BALUN as shown in Figure 1 (c) port 3 combines differential input signals from port 1 and port 2. A high performance BALUN design is critical for integrating the single-end and differential ends. Bandwidth, phase and magnitude imbalances are all the important issues in the BALUN design.

III. THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to

control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and commonly used with negative feedback [6]. The symbol of OTA device shown in Figure 2 and a schematic of an OTA that used in this work is shown in Figure 3.

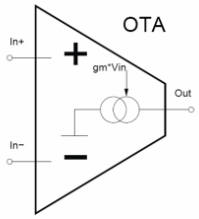

Figure 2. Symbolic of Operational Transconductance Amplifier (OTA)

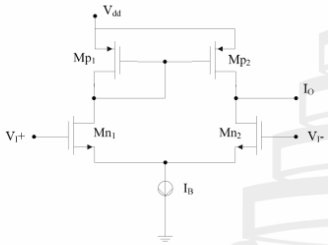

Figure 3. Schematic diagrams of operational transconductance amplifier

For calculation, the ideal transfer characteristic of OTA is

$$\mathrm{I}_{\mathrm{out}} = g_m\left(V_{In+} - V_{in-}\right). \quad (1)$$

or, by taking the pre-computed difference as the input,

Therefore $$\mathrm{I}_{\mathrm{out}} = g_m V_{In}. \quad (2)$$

IV. CIRCUIT DESIGN

To build the OTA based Active BALUN shown in Figure 3, OTA 1 and OTA 2 are used as a power-splitter. Unbalanced signal is applied to OTA 1 positive (+) input and OTA 2 negative (-) input and connected to another differential OTA 1(-) ,2(+) input to ground. OTA 2 worked as phase inverter. OTA 3 and OTA 4 used as pre-load function to adjust output by increasing or decreasing bias current.

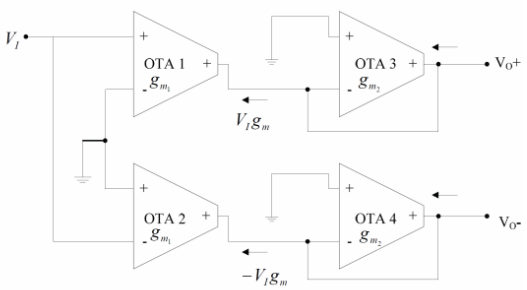

Figure 4. A schematic of power-splitted Active BALUN that used OTA

From Figure 4, the equation to approximate V_O^+ is analyzed via the nodal analysis, which gives

$$V_I g_{m_1} - V_O^+ g_{m_2} = 0. \quad (3)$$

Therefore $$V_O^+ = V_I \frac{g_{m_1}}{g_{m_2}}. \quad (4)$$

In the same manner, the equation for V_O^- is approximated as

$$\left(-V_I g_{m_1}\right) + \left(-V_O^- g_{m_2}\right) = 0. \quad (5)$$

Therefore $$V_O^- = -V_I \frac{g_{m_1}}{g_{m_2}}. \quad (6)$$

From equation (4) and (6), the balance output at V_O is characterized as:

$$V_O = V_I\left(\frac{2g_{m_1}}{g_{m_2}}\right). \quad (7)$$

The relation of both transconductances must be satisfied with the following equation in order to obtain a unity gain BALUN.

$$g_{m_2} = 2g_{m_1}. \quad (8)$$

That makes the input and output equal in power.

$$V_O \cong V_I. \quad (9)$$

V. SIMULATION RESULTS

To verify the validity of the proposed BALUN, the output voltage was simulated as a function of the frequency using HSPICE 2007.3 with the AMS 0.35 BiCMOS process model. The output magnitudes are shown in Figures 5, 7 and 9 where the solid line indicates positive output and the dotted line for negative input. Figures 6, 8 and 10 show the differential signal between output and input. This simulation used a small sine wave signal input of 10 mV PP at 10 MHz and current bias of OTA 1 and OTA2 are 75 µA. The tunable current of OTA 3 and OTA 4 are in steps of 100 µA, 200 µA and 300 µA to show the tunable output magnitude. The results of the different frequency ranges and phase imbalances are shown in Figure 11 and Figure 12 which current bias OTA 1 and OTA 2 are 75 µA and current bias of OTA 3 and OTA 4 are 300 µA. As can be seen in Figure 11 and Figure 12, the operation of the proposed BALUN is in the 1Hz – 100MHz frequency range. The amplitude difference of both voltages is less than 0.02 dB and the phase values are out of phase over the frequency range.

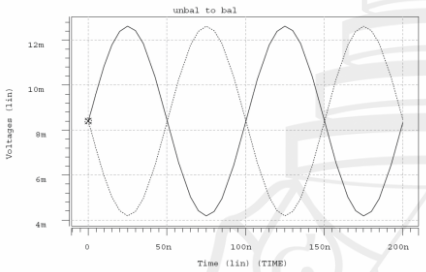

Figure 5. Result of 100 µA current bias for OTA 3 and OTA 4 with output from V_O^+ and V_O^-.

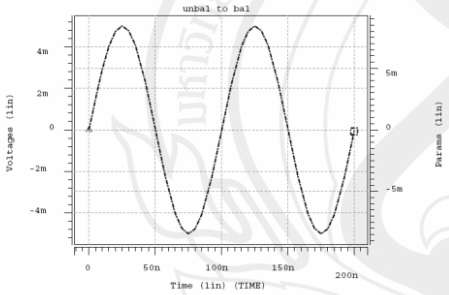

Figure 6. Result of 100 µA current bias for OTA 3 and OTA 4 with voltage output from differential output compared to input.

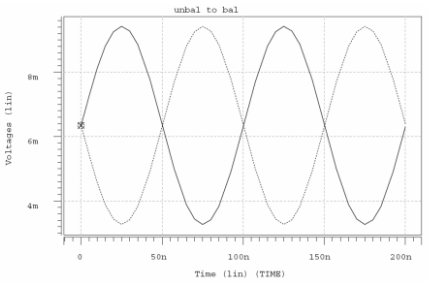

Figure 7. Result of 200 µA current bias for OTA 3 and OTA 4 with output from V_O^+ and V_O^-.

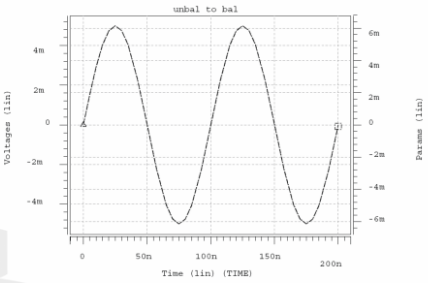

Figure 8. Result of 200 µA current bias for OTA 3 and OTA 4 with output voltage from differential output compared to input.

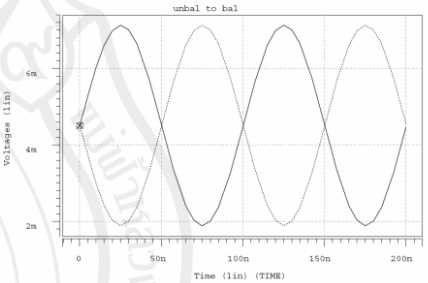

Figure 9. Result of 300 µA current bias for OTA 3 and OTA 4 with output from V_O^+ and V_O^-.

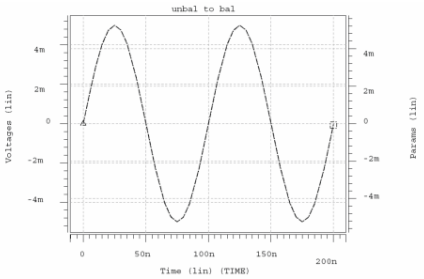

Figure 10. Result of 300 µA current bias for OTA 3 and OTA 4 with output voltage from differential output compared to input.

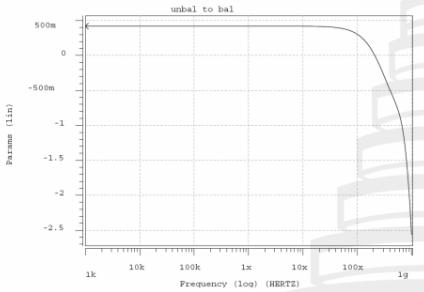

Figure 11. Result of 300 µA current bias for OTA 3 and OTA 4 with voltage differential output in 1 GHz frequencies range in dB .

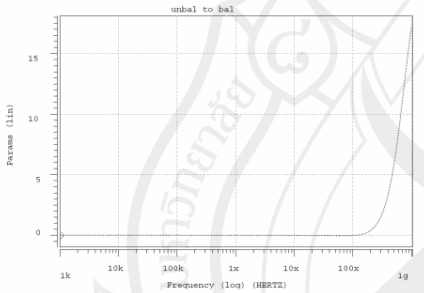

Figure 12. Result of 300 µA current bias for OTA 3 and OTA 4 with phase imbalance of differential output.

VI. CONCLUSION

This research work proposed the new structure of active OTA BALUN based on MOSFET technology. The numbers of transistors in the circuit are 16 MOS transistors, which is less than the number of 48 transistors that are used in CCCII Active BALUN [4, 7]. As shown in the simulated result, the proposed OTA based Active BALUN can be operated in the frequency range from 1 Hz to 100 MHz. The amplitude imbalance is less than 0.02dB over the operating frequency. The problem of the limited frequency is due to the characteristic of AMS 0.35µ MOSFET model issued over ten years ago. This structure can be a significant candidate in BALUN applications with present day high frequency CMOS process.

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APPENDIX C

Active Tunable Nanoscale CMOS BALUN Based on Operational Transconductance Amplifier

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***Abstract*— In modern communication systems, the signal splitter and combiner called BALUN (BALance to UNbalance) is required to interface a single ended device with a differential ended device. Most active BALUN deploy passive elements which cannot be tuned and requires large area in the integrated circuit. Though there is the controllable BALUN based on BiCMOS CCCII, the implementing circuit is quite large in transistor count and the cost of BiCMOS is very expensive. In this work, the new active BALUN based on CMOS OTA is proposed. By adjusting the transconductance of the composed OTAs, the characteristics of BALUN can be tuned electronically. Normally the size of the OTA is half of the size of the CCCII in transistor count. Therefore, the size of proposed structure is theoretically half of the CCCII counterpart. The design structure is simulated in the HSPICE based on the 90nm IBM RF-CMOS process parameters extracted by MOSIS. The result shows that the proposed structure can be a fair alternative in BALUN design via adequate compatibility of BALUN characteristics such as power-splitting, power-combination and phase inverting.**

Keywords-component; Operational Transconductance Amplifier, Active BALUN, CMOS

I. INTRODUCTION

Nowadays, most transceivers are composed of both single ended (SE) and differential ended (DE) components. Therefore, converter circuit call BALance to UNbalance (BALUN) converter is usually needed. Most BALUN designs are based on passive components [1], BJT [2], and BiCMOS[3]. Though these designs work well on their own, most transceivers are favored to be fabricated based only on complementary MOS (CMOS) to be placed among various digital functions. In addition, ability in tuning electronically is also a good option in a BALUN [4] to cover error in gain matching that is likely to be occurred with quite high probability in practical systems.

Interestingly, the operational transconductance amplifier (OTA) simulating voltage-controlled current source (VCCS) [5] is one of the favorite active analogue devices because it transconducatance can be tuned electronically via bias current. Therefore, key properties of its applications can be easily tuned via single or multiple bias current. In addition, the OTA is usually small compared to the current controlled current conveyor (CCCII) which is formerly composing a tunable active BALUN [4]. In this paper, the novel active nanoscale CMOS BALUN is proposed based on OTAs. The proposed circuit will be easily placed in a mixed signal chip because it requires no passive elements and no different type of transistors.

II. THE BALUN

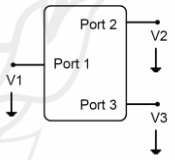

Figure 1. Structural of BALUN

A BALUN is a device for interfacing a single-ended signal with differential-ended signal as show in Figure 1. A single-ended device is connected to the port 1 and a differenctial-ended device is connected to the port 2 and 3. If the input is single ended, the output at port 2 and 3 provides equal half power but 180º difference in phase. For signal combining, port 1 is the output and port 2 and 3 are the input. Figure 2 shows connection schemes for both types of BALUN. A high performance BALUN design is critical for integrating the single-end and differential ends devices. Bandwidth, phase and magnitude imbalances are all the important issues in the BALUN design.

magnitude imbalances are all the important issues in the BALUN design.

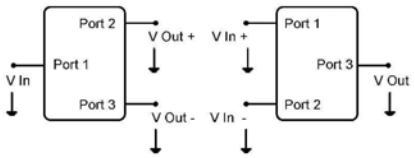

Figure 2. Power-splitted and power-combined BALUN

III. THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and commonly used with negative feedback [6]. The symbol of OTA device is shown in figure 3 and the schematic of OTA utilized in this work is showed in Figure 4.

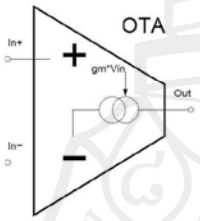

Figure 3. Symbolic of Operational Transconductance Amplifier (OTA)

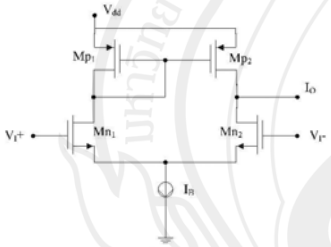

Figure 4. Schematic diagrams of operational transconductance amplifier

For calculation, the ideal transfer characteristic of OTA is

$$I_{out} = g_m\left(V_{In+} - V_{in-}\right) \quad (1)$$

or, by taking the pre-computed difference as the input,

$$I_{out} = g_m V_{In} \quad (2)$$

IV. CIRCUIT DESIGN

To build the OTA based power-splitter active BALUN shown in Figure 5, OTA 1 and OTA 2 are use as power-splitter and phase inverting. Unbalanced signal is put to OTA 1 positive (+) input and OTA 2 negative (-) input and connecting another differential input to ground. OTA 2 worked as phase inverting. OTA 3 and OTA 4 used as pre-load function to adjust output by increasing or decreasing bias current.

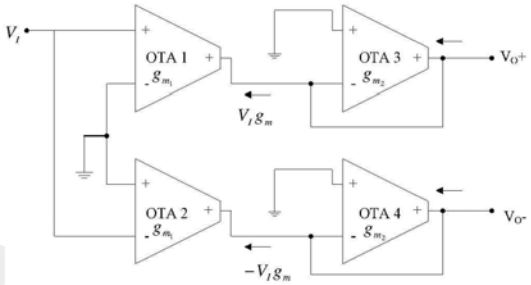

Figure 5. A schematic of power-splitted Active BALUN that used OTA

From figure 5, the equation to approximate V_O^+ is analyzed via the nodal analysis, which gives

$$V_I g_{m_1} - V_O^+ g_{m_2} = 0 \quad (3)$$

Therefore

$$V_O^+ = V_I \frac{g_{m_1}}{g_{m_2}} \quad (4)$$

In the same manner, the equation for V_O^- is approximated as

$$\left(-V_I g_{m_1}\right) + \left(-V_O^- g_{m_2}\right) = 0 \quad (5)$$

Therefore

$$V_O^- = -V_I \frac{g_{m_1}}{g_{m_2}} \quad (6)$$

From equation (4) and (6), the balance output at V_O is characterized as:

$$V_O = V_I\left(\frac{2g_{m_1}}{g_{m_2}}\right) \quad (7)$$

The relation of both transconductances must be satisfied the following equation in order to obtain a unity gain BALUN.

$$g_{m_2} = 2g_{m_1} \quad (8)$$

Which make the input and output equal in power.

$$V_O \cong V_I \quad (9)$$

The structure for a signal combining BALUN is shown in fig. 6. The OTA 1 is used as input stage and the OTA 2 acts as pre-load device.

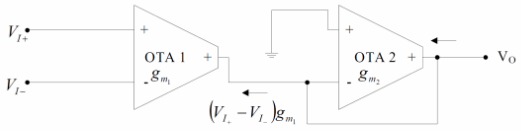

Figure 6. A schematic of power-combined Active BALUN that used OTA

The nodal analysis is taken at the output of OTA 1 which gives:

$$\left(V_{I_+} - V_{I_-}\right)g_{m_1} - V_O g_{m_2} = 0 \qquad \textbf{(10)}$$

Therefore

$$V_O = \left(V_{I_+} - V_{I_-}\right)\frac{g_{m_1}}{g_{m_2}} \qquad \textbf{(11)}$$

To make input and output power equal, the following criteria must be met.

$$g_{m_2} = g_{m_1} \qquad \textbf{(12)}$$

Therefore, single ended output power is as the same as the differential input power

$$V_O \cong \left(V_{I_+} - V_{I_-}\right) \qquad \textbf{(13)}$$

V. Simulation Results

To verify the validity of the proposed BALUN, both transient and frequency response of signal splitter were simulated by HSPICE 2007.3 based on the 90nm IBM RF-CMOS process extracted by the MOSIS. The bias currents are 80 µA for OTA 1 and 2, 172 µA for OTA 3 and 4. The frequency responses are shown in Figure 7. Phase imbalance is shown in Figure 8. And the transient response from 2.5GHz 10mV PP input is plotted in fig. 9. As can be seen in the Figure 7, the operation of the proposed BALUN is approximately in the 1MHz – 15.7GHz bandwidth. The phase value is out of phase over the frequency range. The output of the power-combined BALUN is also simulated with same simulator and MOSFET model. The biases current are 190 µA for both OTAs. The output frequency response is shown in figure 10 and the transient response based on two 2.5GHz 20mV PP out phase input is shown in fig. 11. The magnitude of frequency response is approximately flat to several GHz. With 2.5 GHz test input, the signal combiner shows smooth response with very low offset.

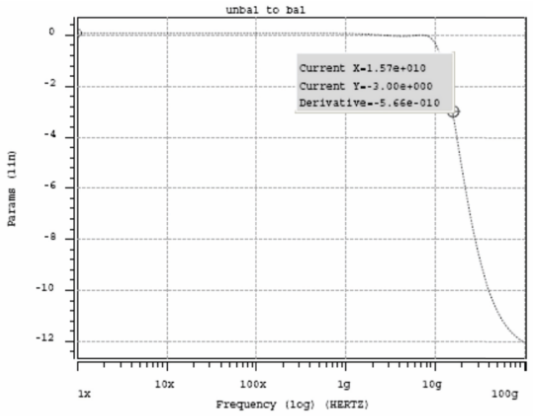

Figure 7. Show frequencies responds and dB from V_o output of power-splitted BALUN, -3dB Bandwidth is15.7GHz

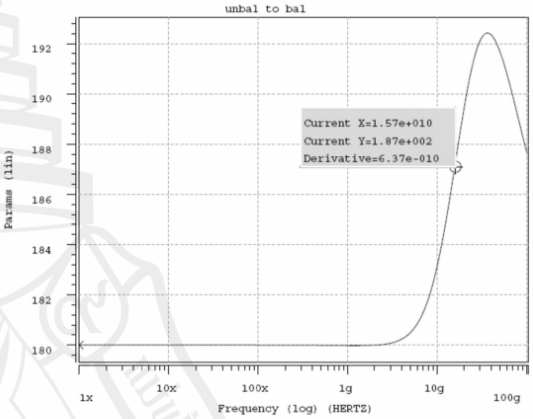

Figure 8. Phase differential 180 degree output from power-splitted BALUN with 7.14º of phase imbalance at -3dB Bandwidth (15.7GHz).

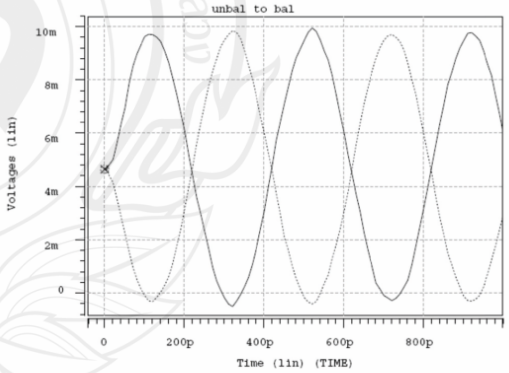

Figure 9. Drifferential output of power splited BALUN transient analysis for input 10mV at 2.5GHz

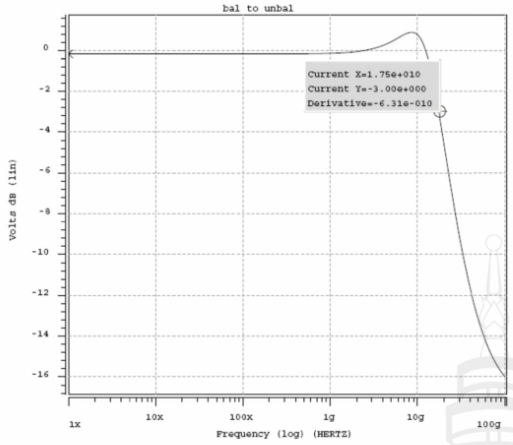

Figure 10. Show frequencies responds and dB from V_o output of power-combined BALUN, -3dB Bandwidth is17.5 GHz

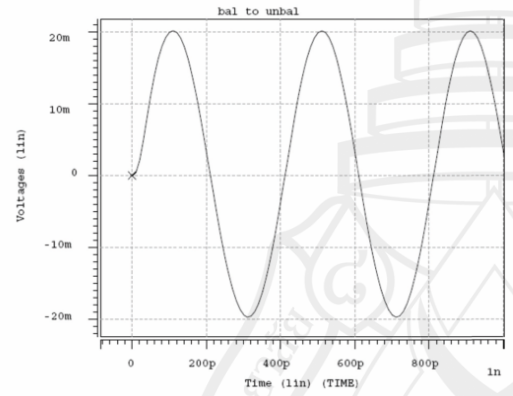

Figure 11. A transient analysis of Combined output of power Combine BALUN for 2 input of 20mV PP which 180 degree out phase at 2.5GHz

VI. CONCLUSION

This research work proposed a new structure of active OTA BALUN in nanoscale based on MOSFET technology. The numbers of transistor in the power-splitting circuit are 16 transistors but only 8 transistors for power combining circuit, which is far less than the number of 48 transistors of the CCCII version [4, 7]. As shown in the simulated result, the proposed OTA based power-splitting active BALUN can be operated in the frequency range from 1 MHz to 15.7 GHz and the power-combining bandwidth is 1 MHz to 17.5 GHz. The phase imbalance of power splitted-BALUN is less than 7.14 degree over the operating frequency.

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